FIG. 1

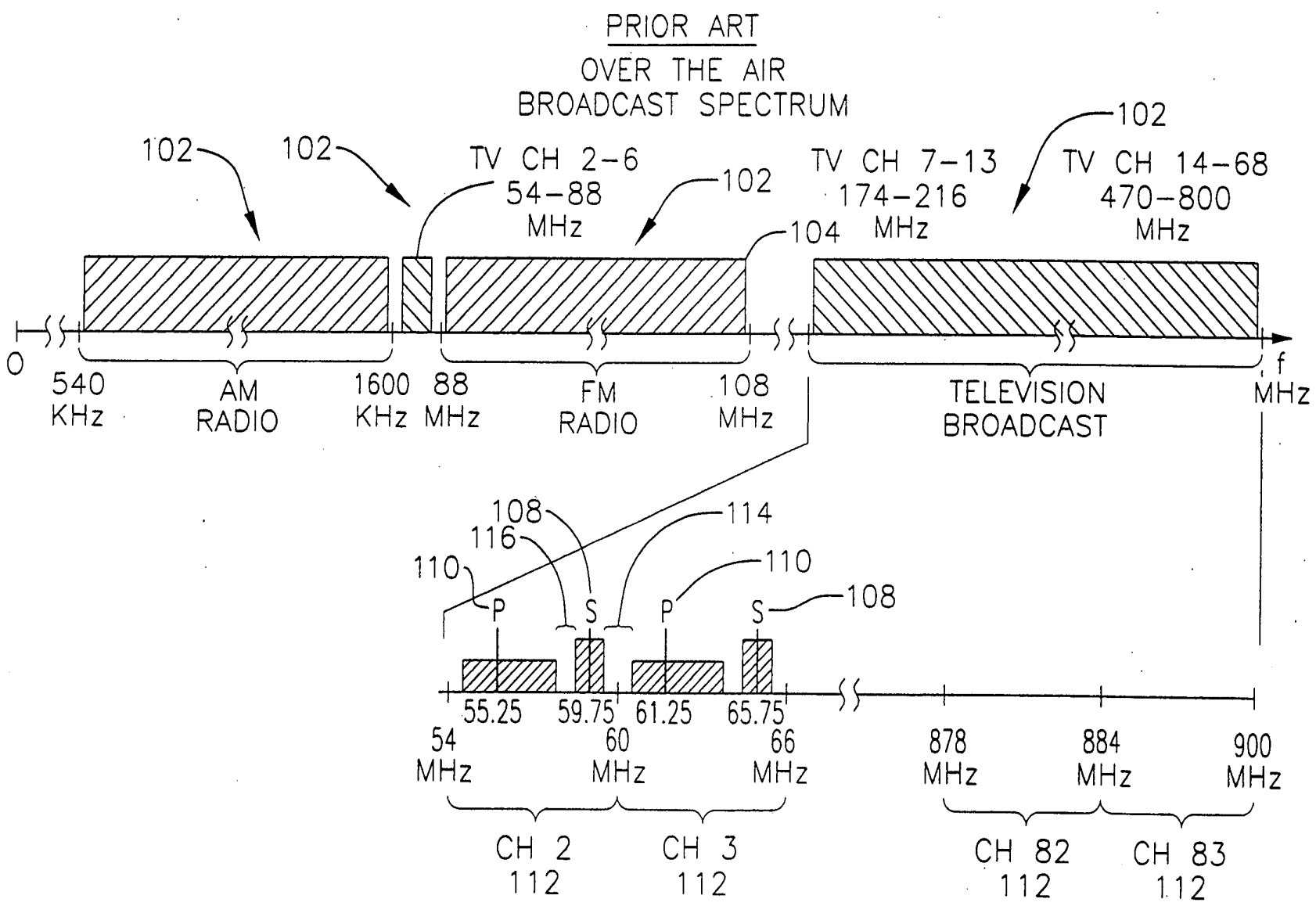

PRIOR ART
OVER THE AIR
BROADCAST SPECTRUM
102
102
TV CH 2-6
54-88
MHz
102
TV CH 7-13
174-216
MHz
102
TV CH 14-68
470-800
MHz
104
0
540
KHz
AM
RADIO
1600
KHz
88
MHz
FM
RADIO
108
MHz
TELEVISION
BROADCAST
f
MHz
108
116
114
110
110
P
S
P
S
108
55.25
59.75
61.25
65.75
54
MHz
60
MHz
66
MHz
878
MHz
884
MHz
900
MHz
CH 2
112
CH 3
112
CH 82
112
CH 83
112

FIG.2

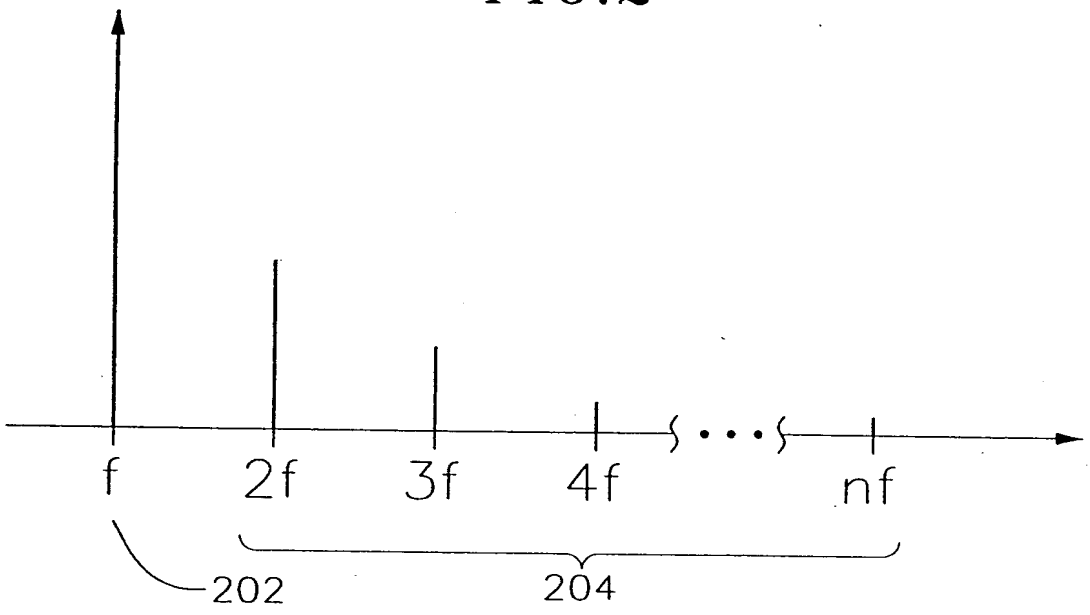


FIG.3
PRIOR ART

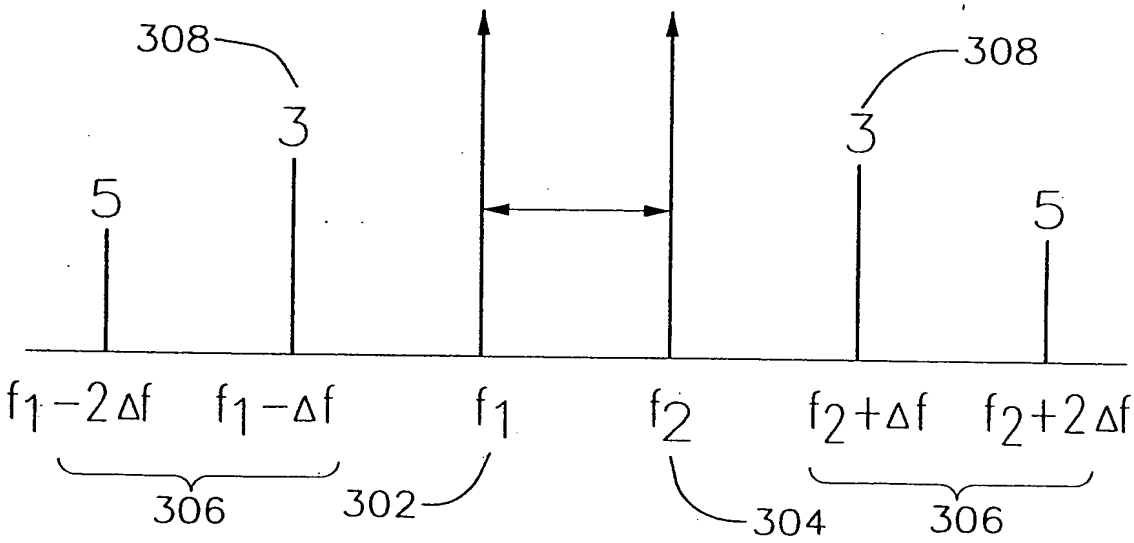


FIG. 4

PRIOR ART

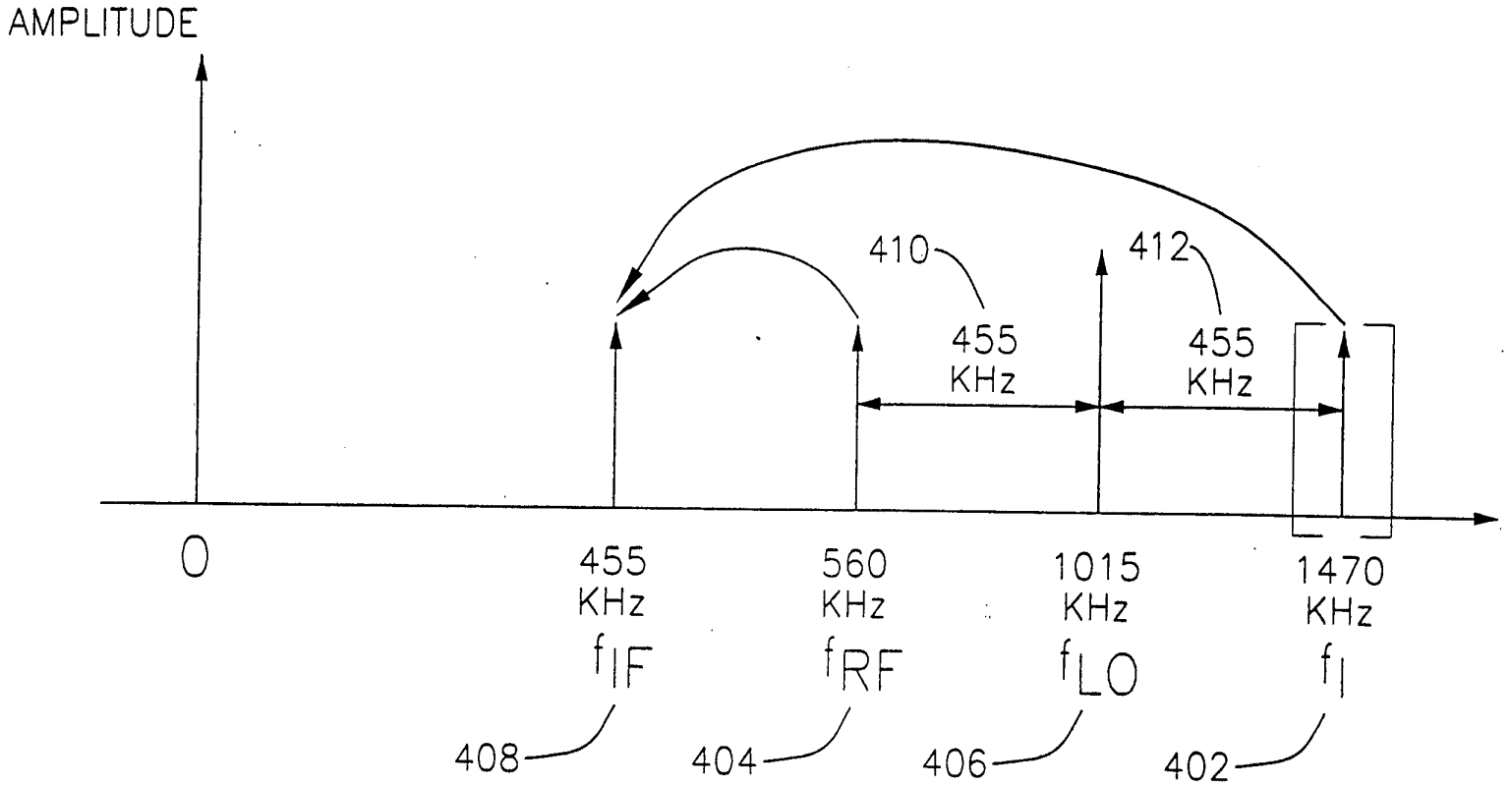
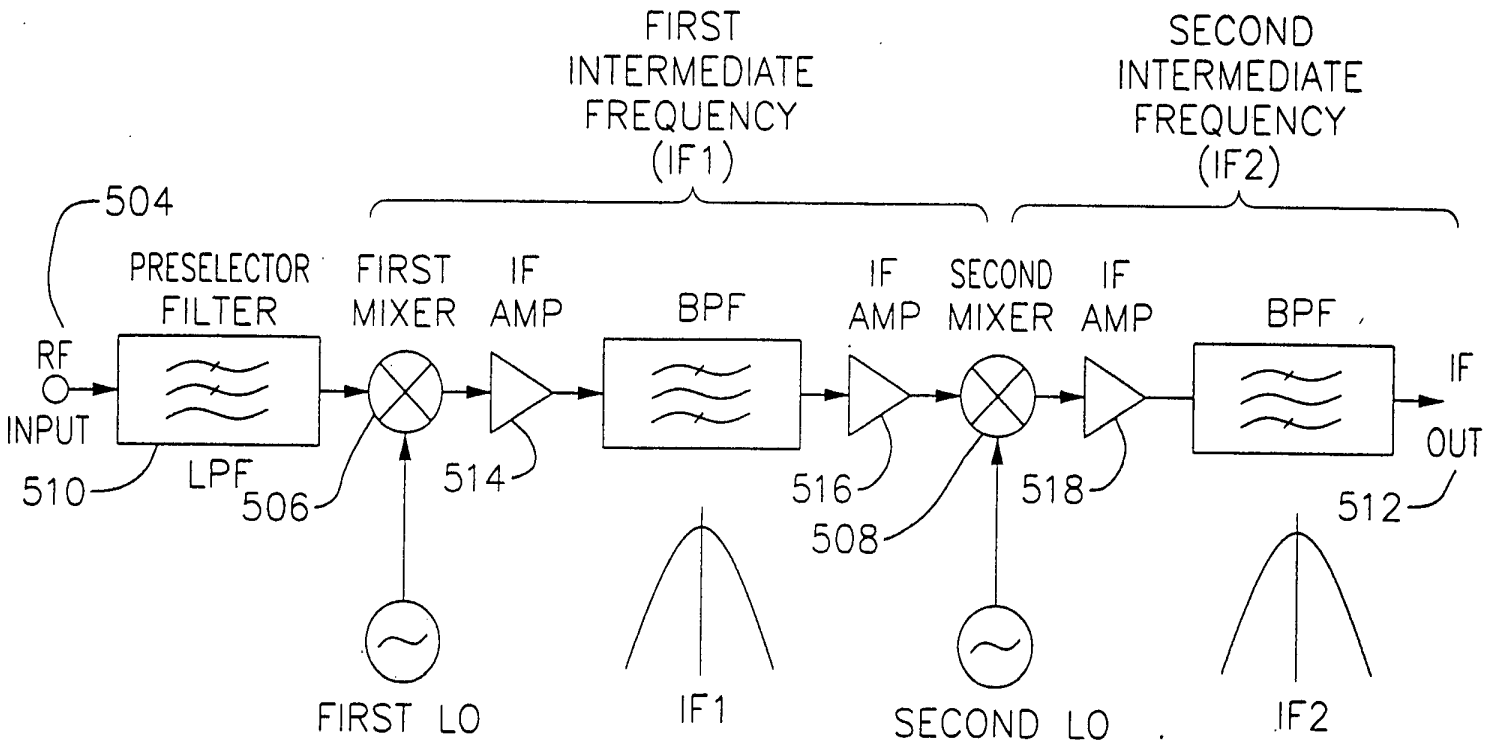


FIG.5

DUAL CONVERSION RECEIVER



IF2<RFINPUT<IF1

FIG. 6

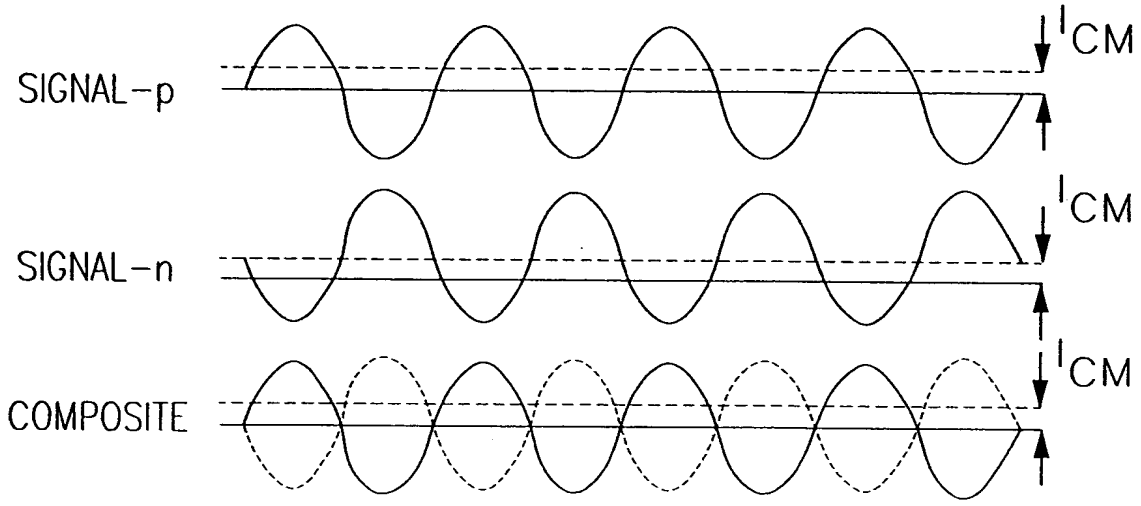

SIGNAL-p
SIGNAL-n
COMPOSITE
I_{CM}
I_{CM}
I_{CM}

FIG. 7

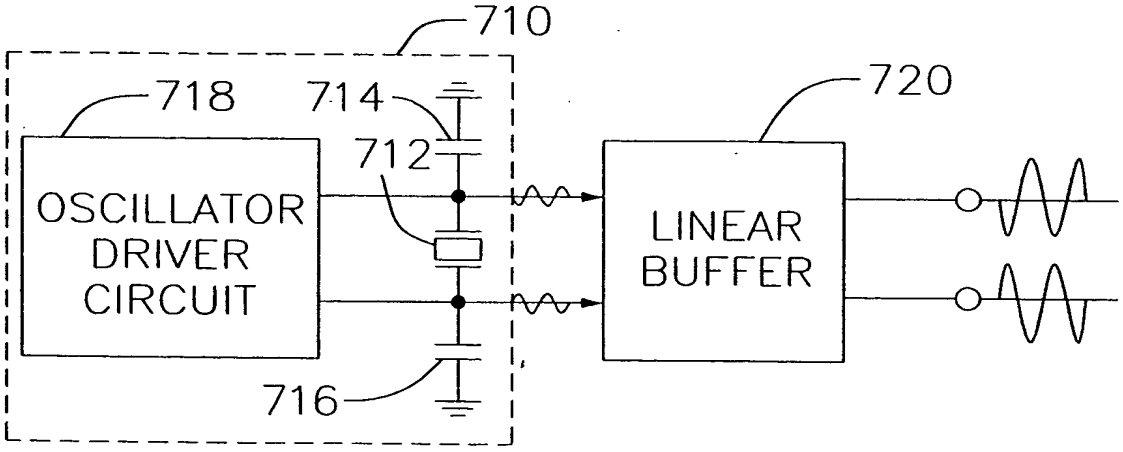

710
718
714
712
720
OSCILLATOR DRIVER CIRCUIT
LINEAR BUFFER
716

FIG. 8

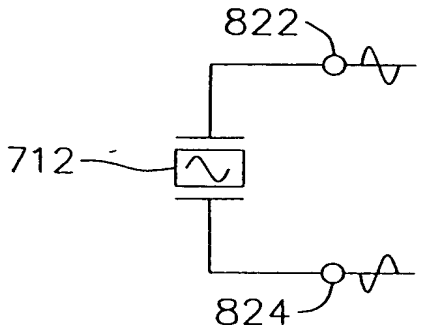


FIG. 9

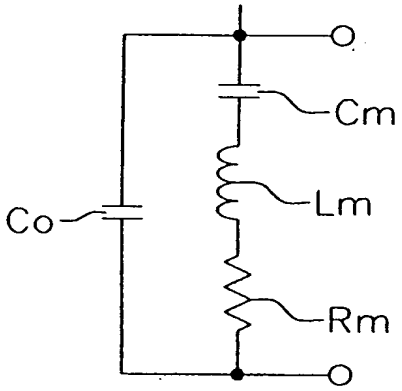


FIG. 10

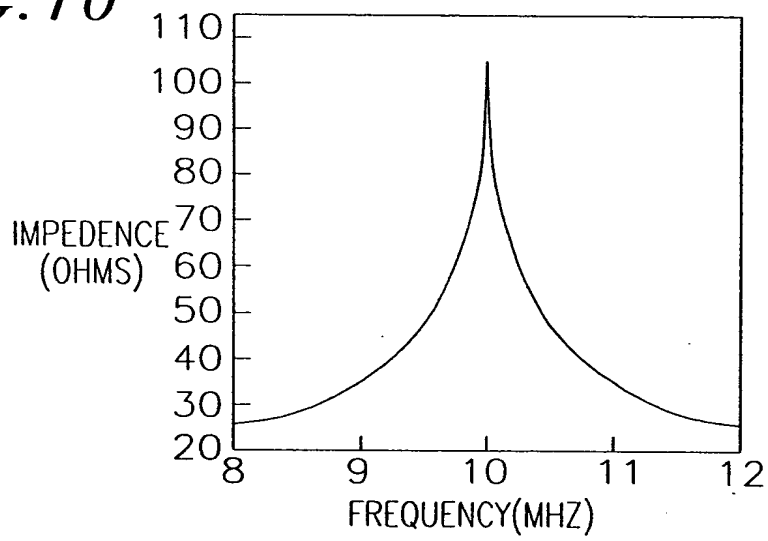


FIG. 11

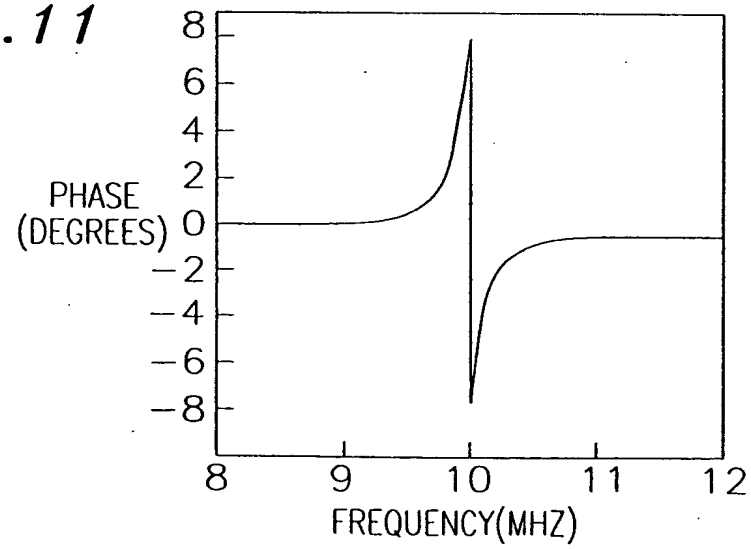


FIG. 12

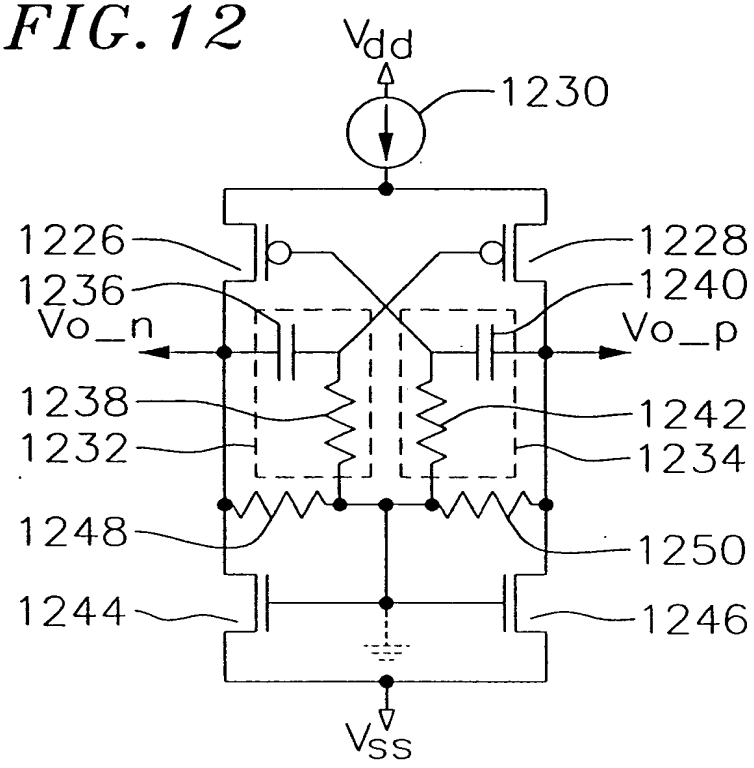

Vdd
1230
1226
1228
1236
1240
Vo_n
Vo_p
1238
1242
1232
1234
1248
1250
1244
1246
Vss

FIG. 13

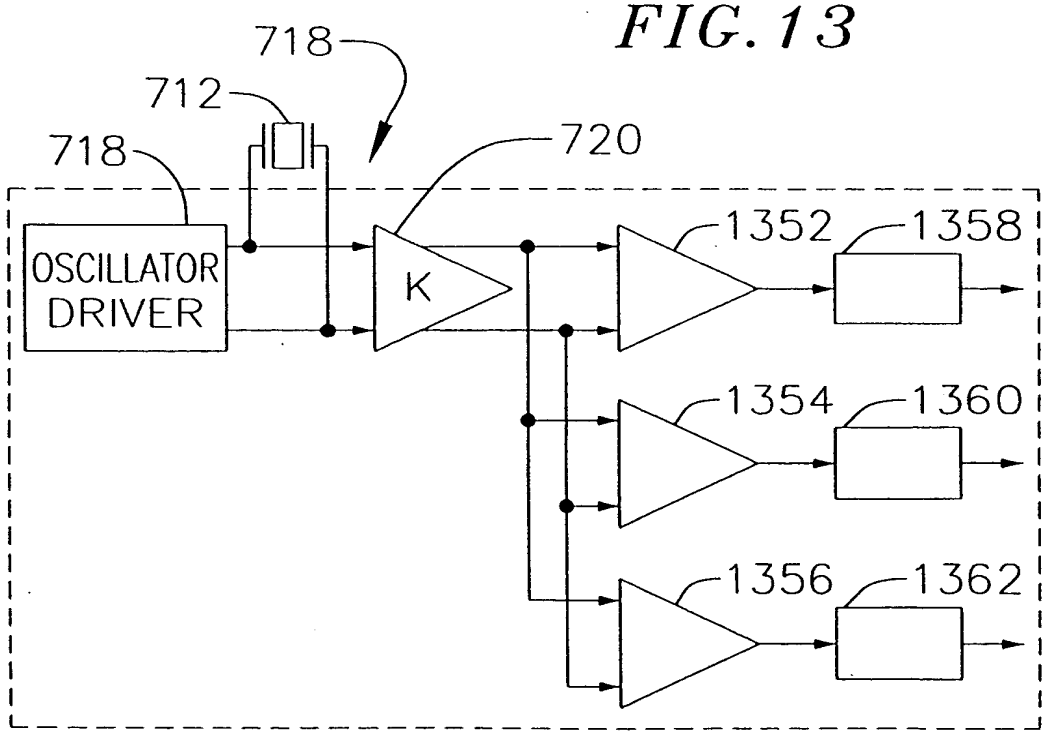

718
712
718
720
OSCILLATOR DRIVER
K
1352
1358
1354
1360
1356
1362

FIG. 14

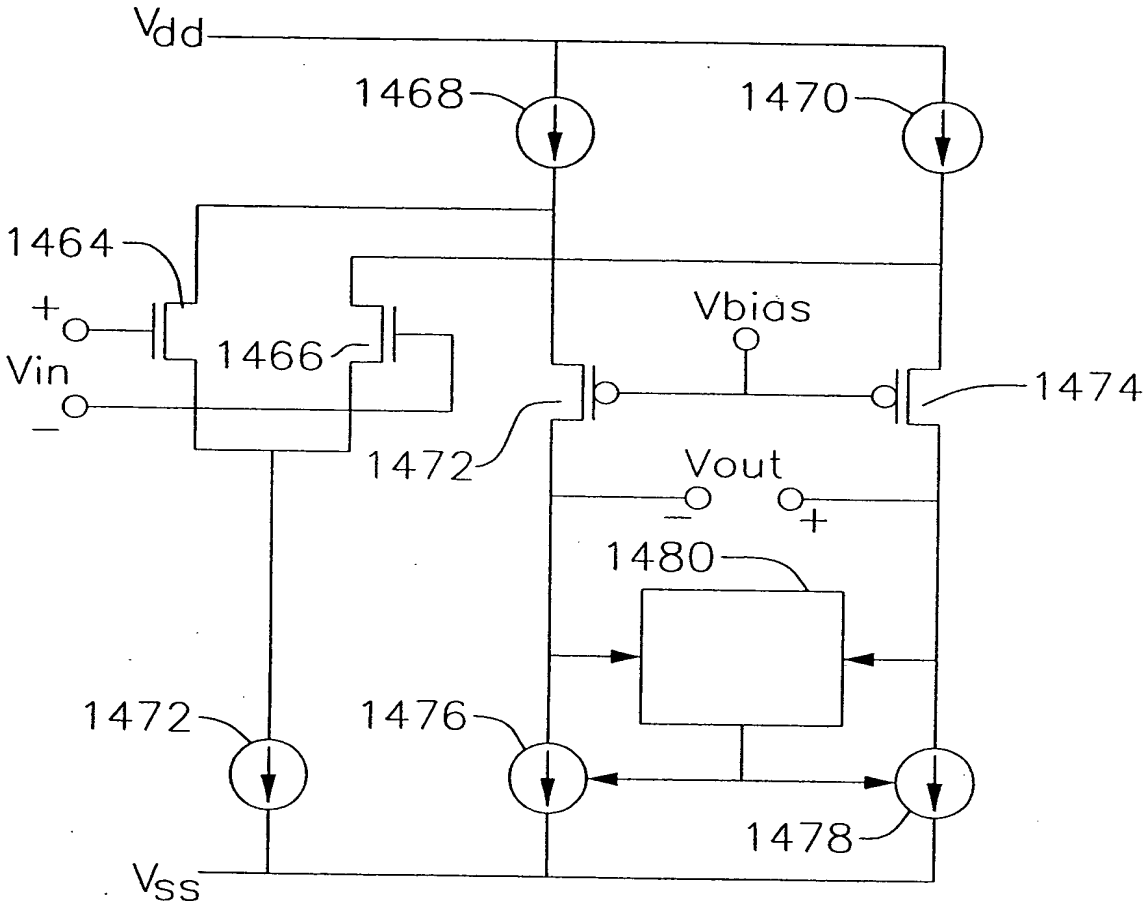

Vdd
1468
1470
1464
+
Vin
−
1466
Vbias
1474
1472
Vout
−
+
1480
1472
1476
1478
Vss

FIG. 15

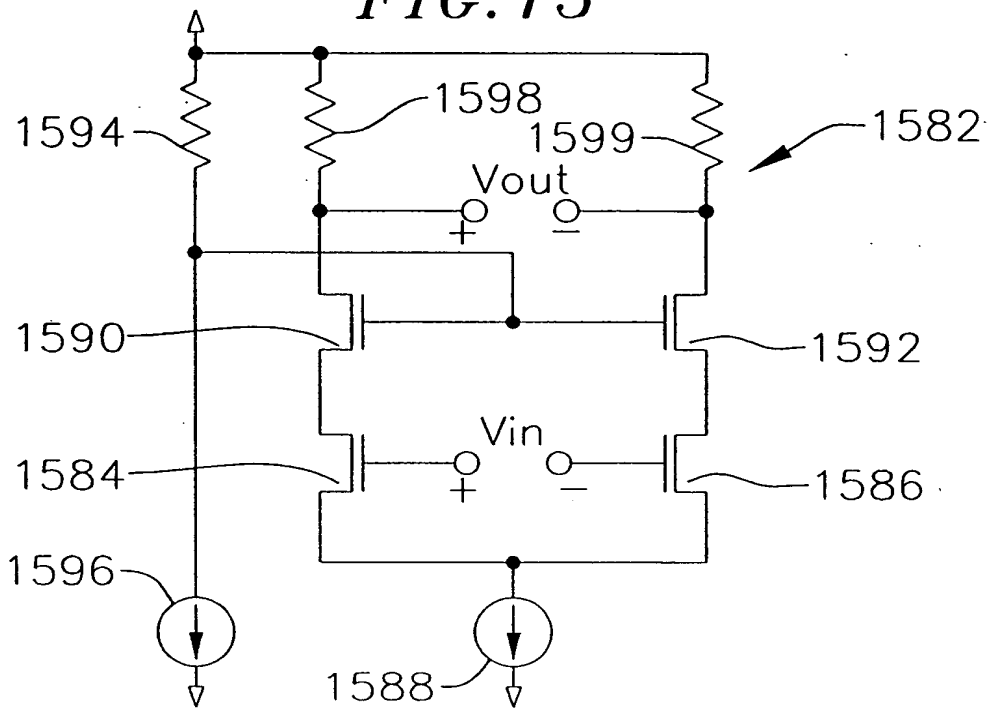

1594
1598
1599
1582
Vout
+
−
1590
1592
Vin
1584
1586
1596
1588

FIG. 16

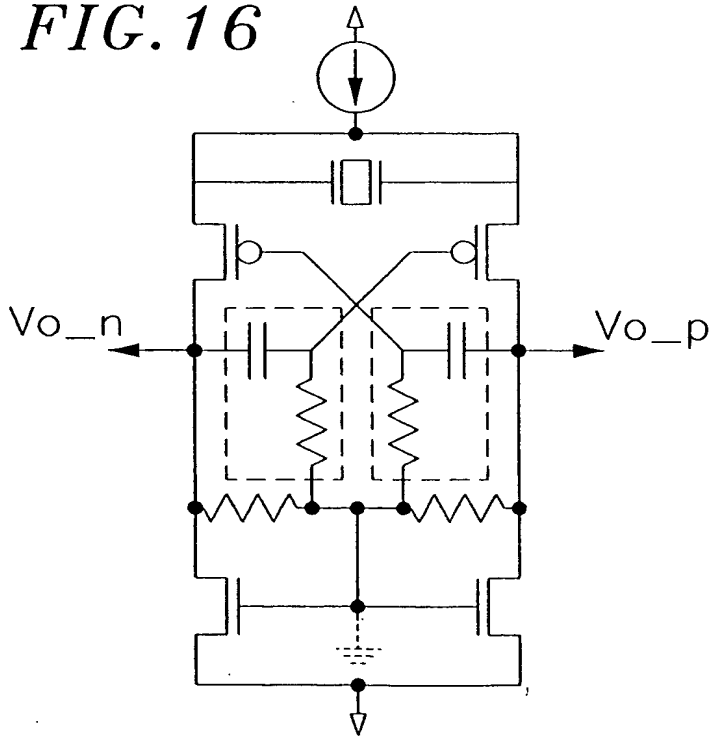

Vo_n
Vo_p

FIG. 17

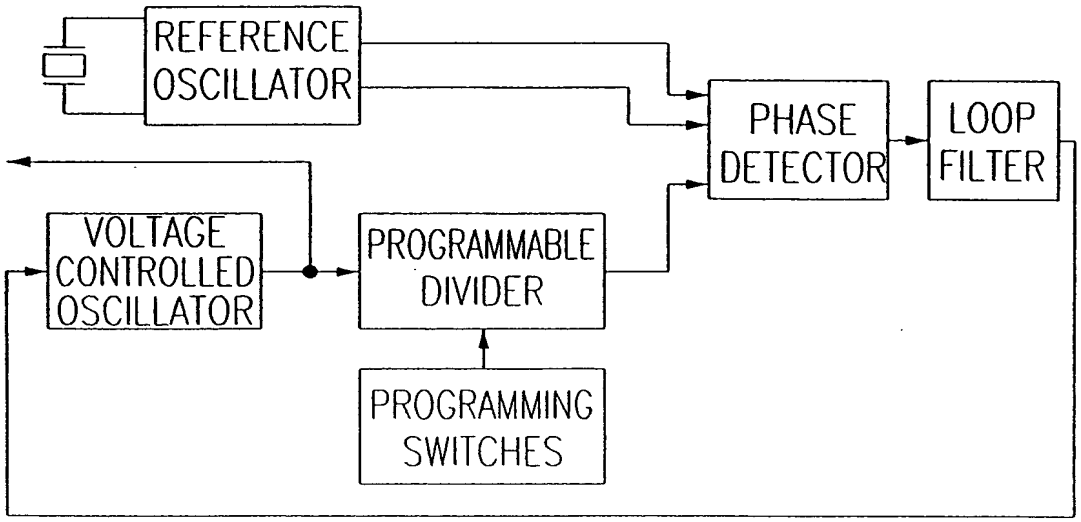

REFERENCE OSCILLATOR
PHASE DETECTOR
LOOP FILTER
VOLTAGE CONTROLLED OSCILLATOR
PROGRAMMABLE DIVIDER
PROGRAMMING SWITCHES

FIG. 18

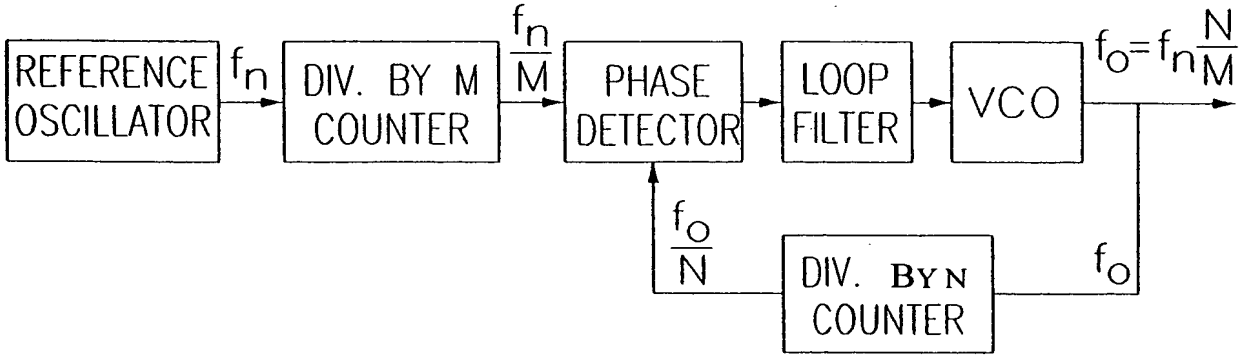

REFERENCE OSCILLATOR
f_n
DIV. BY M COUNTER
$\frac{f_n}{M}$
PHASE DETECTOR
LOOP FILTER
VCO
$f_O = f_n \frac{N}{M}$
$\frac{f_O}{N}$
DIV. BY N COUNTER
f_O

FIG. 19

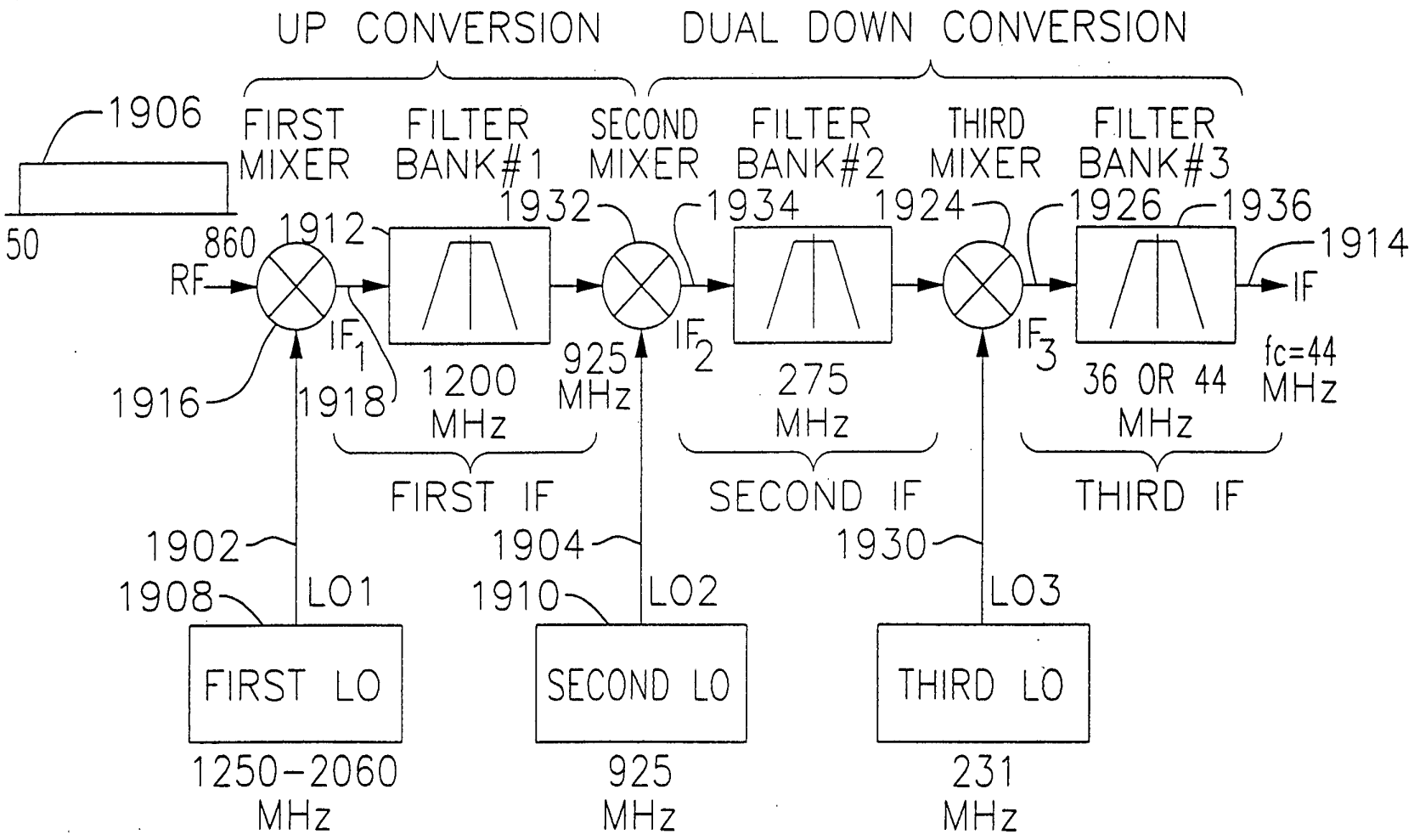
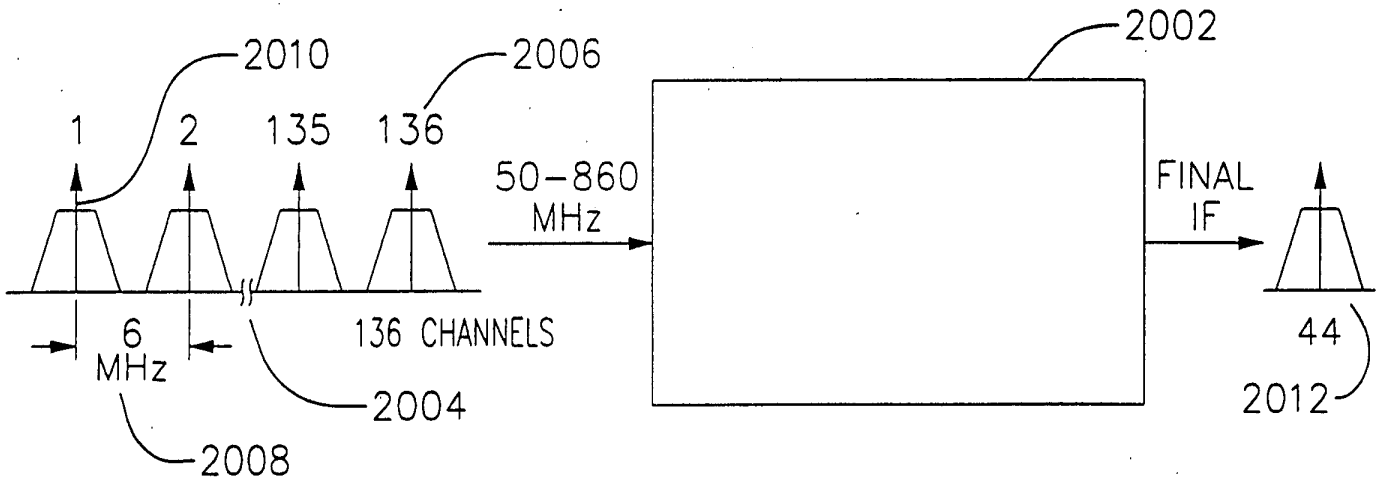

UP CONVERSION
DUAL DOWN CONVERSION
1906
FIRST MIXER
FILTER BANK#1
SECOND MIXER
FILTER BANK#2
THIRD MIXER
FILTER BANK#3
50
860
RF
1912
1932
1934
1924
1926
1936
1914
IF
IF1
IF2
IF3
1916
1918
1200 MHz
925 MHz
275 MHz
36 OR 44 MHz
fc=44 MHz
FIRST IF
SECOND IF
THIRD IF
1902
1904
1930
1908
LO1
1910
LO2
LO3
FIRST LO
SECOND LO
THIRD LO
1250-2060 MHz
925 MHz
231 MHz

FIG.20


2010
2006
2002
1
2
135
136
50–860
MHz
FINAL
IF
6
MHz
136 CHANNELS
44
2004
2012
2008

PPL Xtal REFERENCE=10MHz
LO-1, 10MHz FREQUENCY STEPS
LO-2, 100kHz FREQUENCY STEPS

FIG.21

44MHz IF

TABLE OF FREQUENCIES BASED ON COARSE/FINE PLL SOLUTION:

NOTE
- LO-2 REF=100KHz
  SO DIVIDE RANGE=9216 TO 9280

Frf (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1 (MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	1200	1204	1198	1202	1196	1200	1204	1198	1202	1196	1200	1204	1198	1202	"	1196	1200
LO-2 (MHz)	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	"	921.6	924.8
IF-2 (MHz)	275.2	276	274.8	275.6	274.4	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	"	274.4	275.2
LO-3 (MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3 (MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

PPL Xtal REFERENCE=10MHz
LO-1, 10MHz FREQUENCY STEPS
LO-2, 100kHz FREQUENCY STEPS

FIG.22

36MHz IF

TABLE OF FREQUENCIES BASED ON COARSE/FINE PLL SOLUTION:

NOTE
- LO-2 REF=100KHz
  SO DIVIDE RANGE=9280 TO 9340

Frf (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1 (MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	1200	1202	1204	1196	1198	1200	1202	1204	1196	1198	1200	1202	1204	1196	"	1198	1200
LO-2 (MHz)	931.2	932.8	934.4	928.0	930	931	933	934	928.0	930	931	933	934	928.0	"	929.60	931.2
IF-2 (MHz)	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	"	268.4	268.8
LO-3 (MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3 (MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0

FIG.23

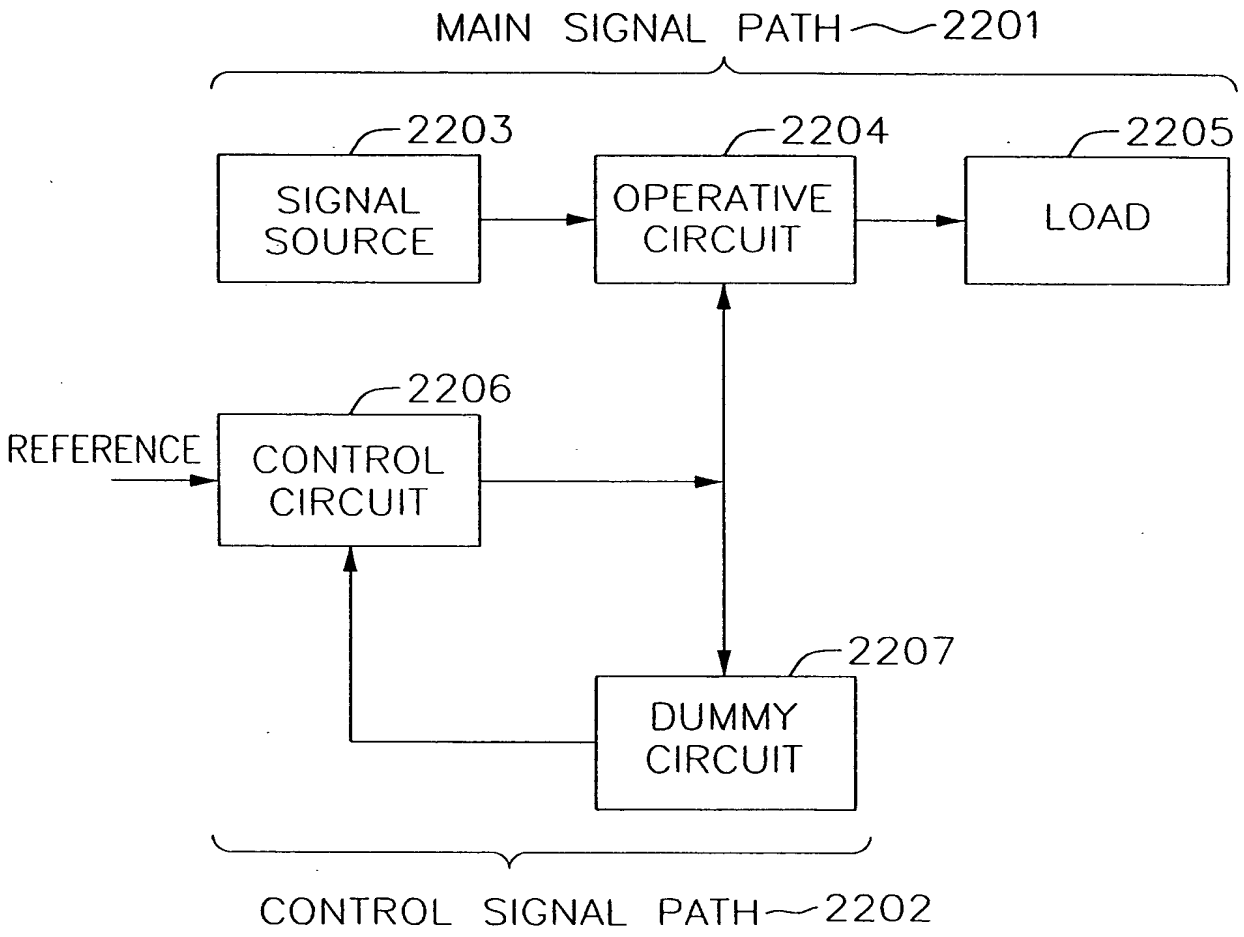
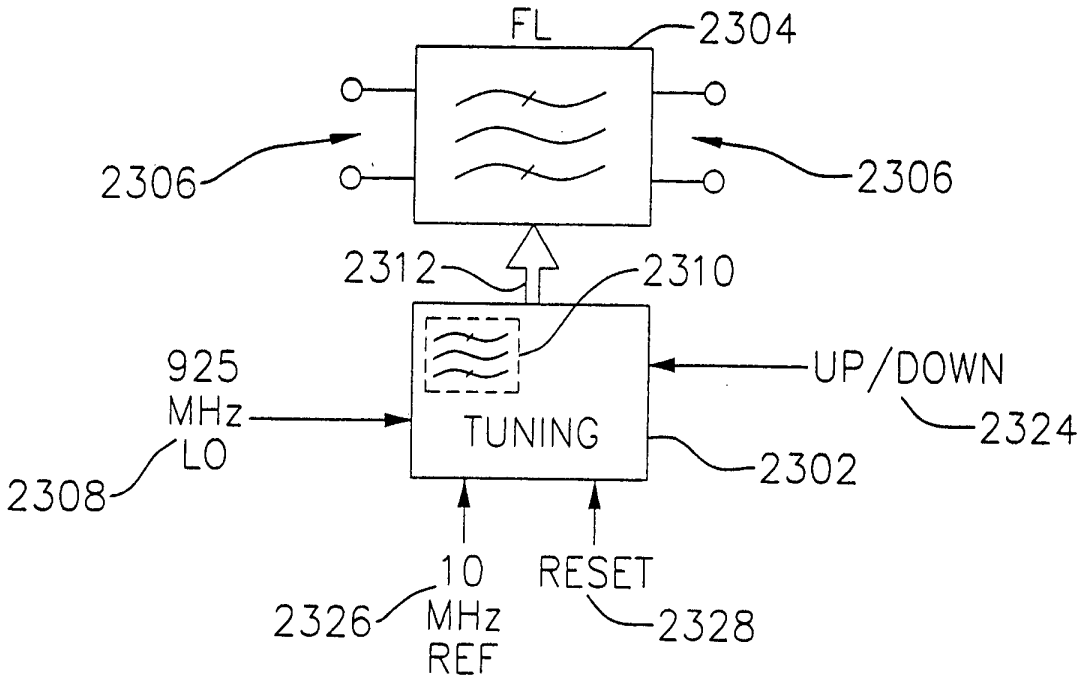

MAIN SIGNAL PATH
2201
2203
2204
2205
SIGNAL SOURCE
OPERATIVE CIRCUIT
LOAD
2206
REFERENCE
CONTROL CIRCUIT
2207
DUMMY CIRCUIT
CONTROL SIGNAL PATH
2202

FIG.24a


FL
2304
2306
2306
2312
2310
925
MHz
LO
2308
TUNING
UP/DOWN
2324
2302
10
MHz
REF
2326
RESET
2328

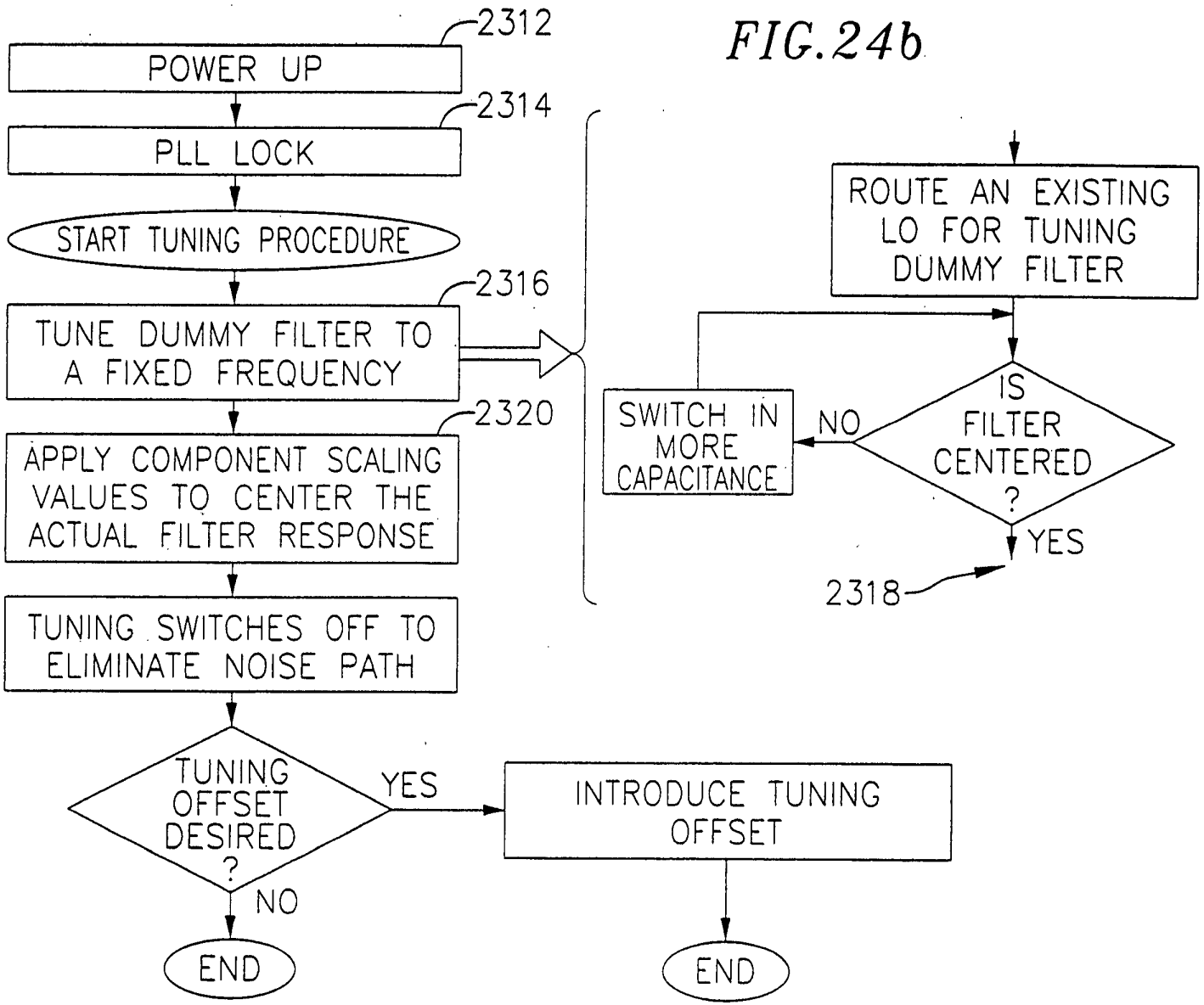

2312
POWER UP
2314
PLL LOCK
START TUNING PROCEDURE
2316
TUNE DUMMY FILTER TO A FIXED FREQUENCY
2320
APPLY COMPONENT SCALING VALUES TO CENTER THE ACTUAL FILTER RESPONSE
TUNING SWITCHES OFF TO ELIMINATE NOISE PATH
TUNING OFFSET DESIRED ?
YES
NO
END
INTRODUCE TUNING OFFSET
END
ROUTE AN EXISTING LO FOR TUNING DUMMY FILTER
IS FILTER CENTERED ?
NO
SWITCH IN MORE CAPACITANCE
YES
2318

FIG.24b

FIG.24c

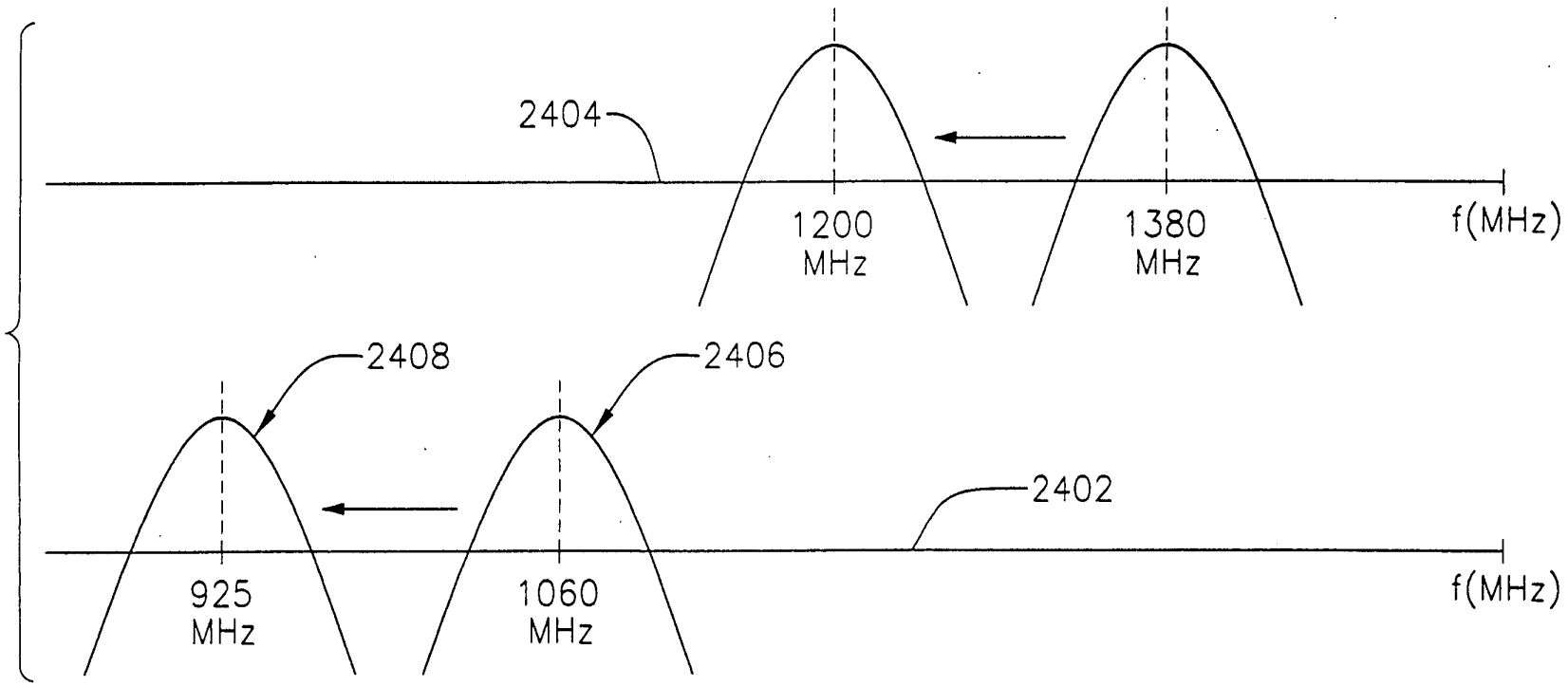

2404
1200
MHz
1380
MHz
f(MHz)
2408
2406
2402
925
MHz
1060
MHz
f(MHz)

FIG.25

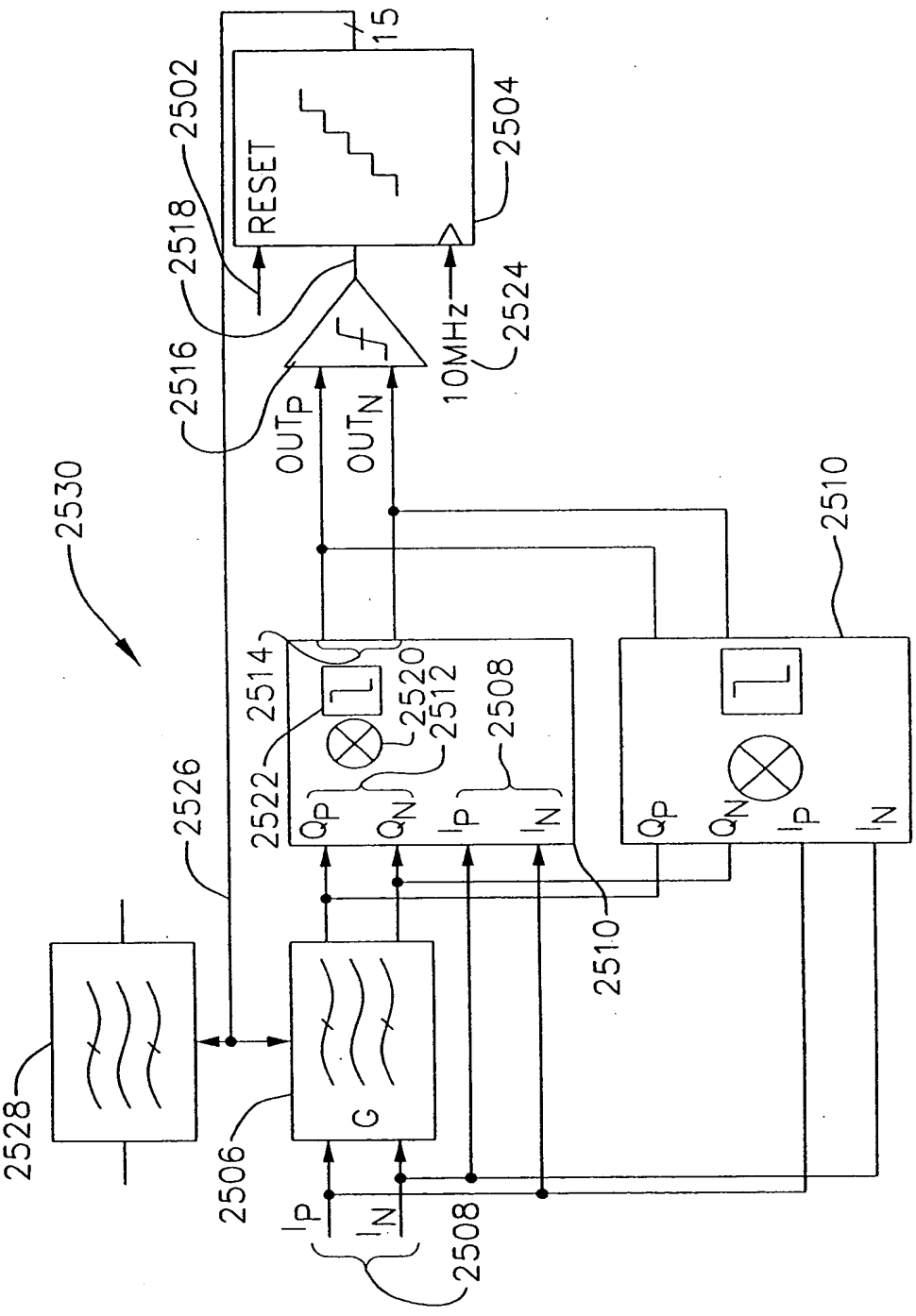

2530
2502
15
RESET
2504
2518
2516
2524
10MHz
OUTP
OUTN
2514
2520
2512
2522
2508
2526
QP
QN
IP
IN
2510
2528
2506
G
2508

FIG.26

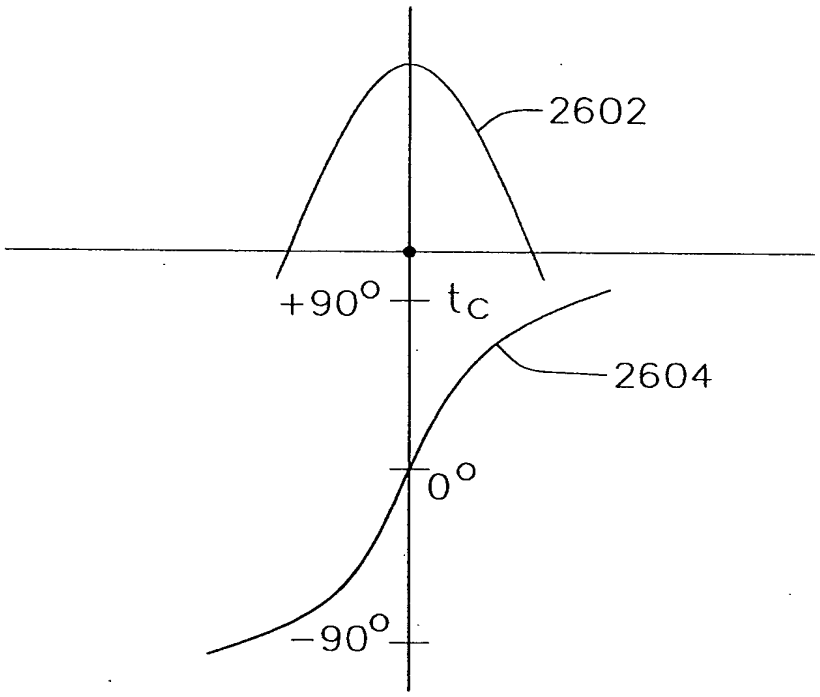


FIG. 27

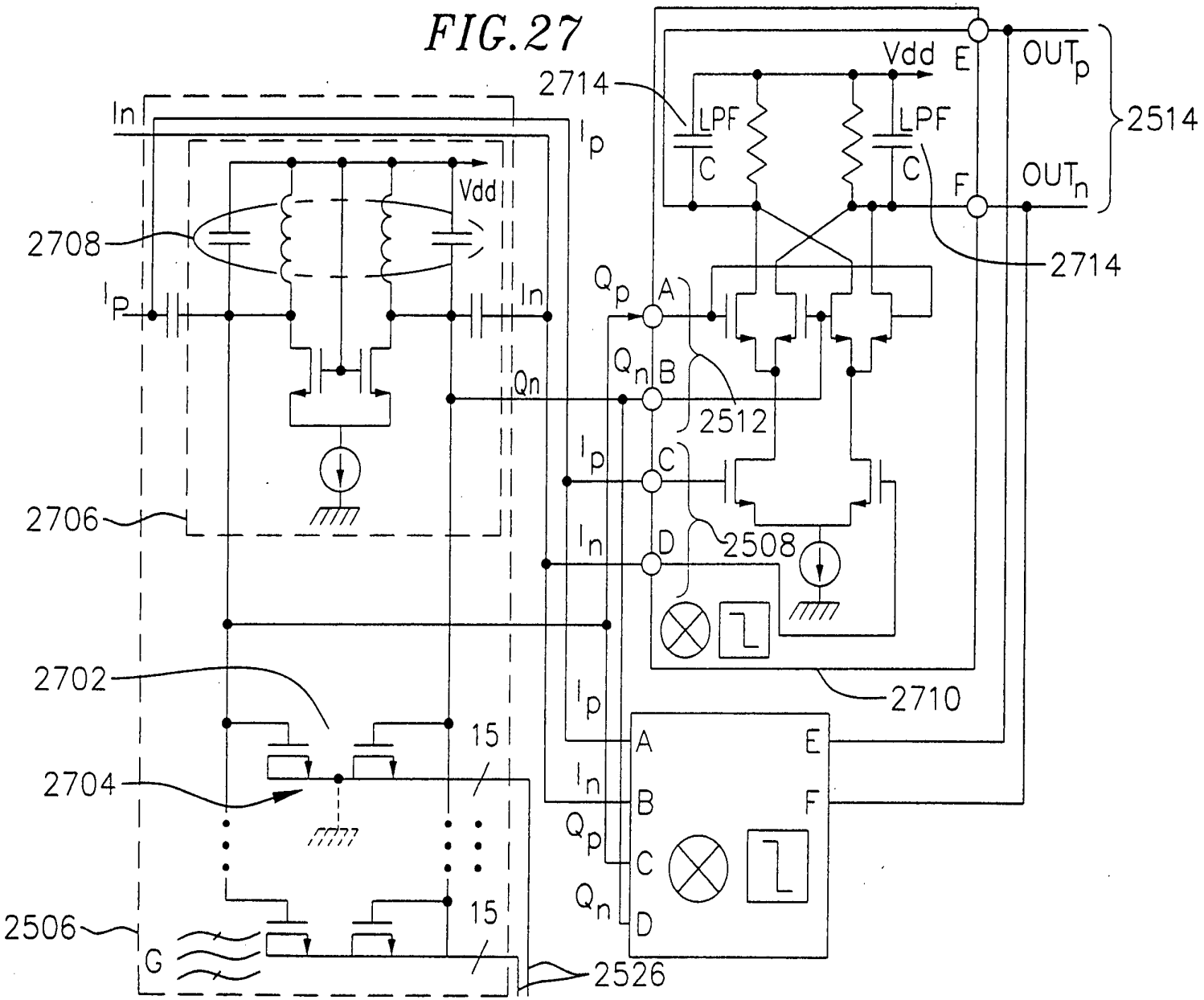

2714
Vdd
E
OUTp
2514
LPF
C
LPF
C
F
OUTn
2714
In
Ip
2708
Vdd
Ip
In
Qp
A
Qn
B
Qn
2512
Ip
C
2706
In
D
2508
2710
2702
Ip
15
A
E
2704
In
B
F
Qp
C
Qn
D
15
2506
G
2526

FIG.28a

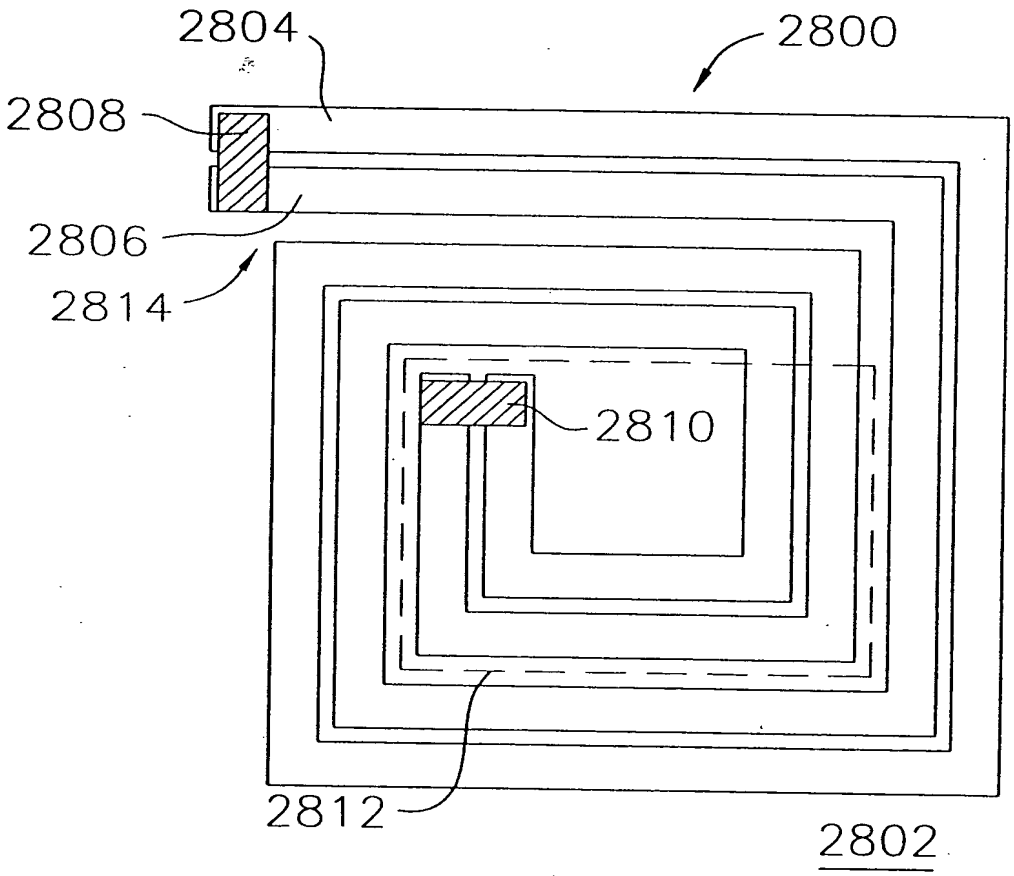


FIG.28b

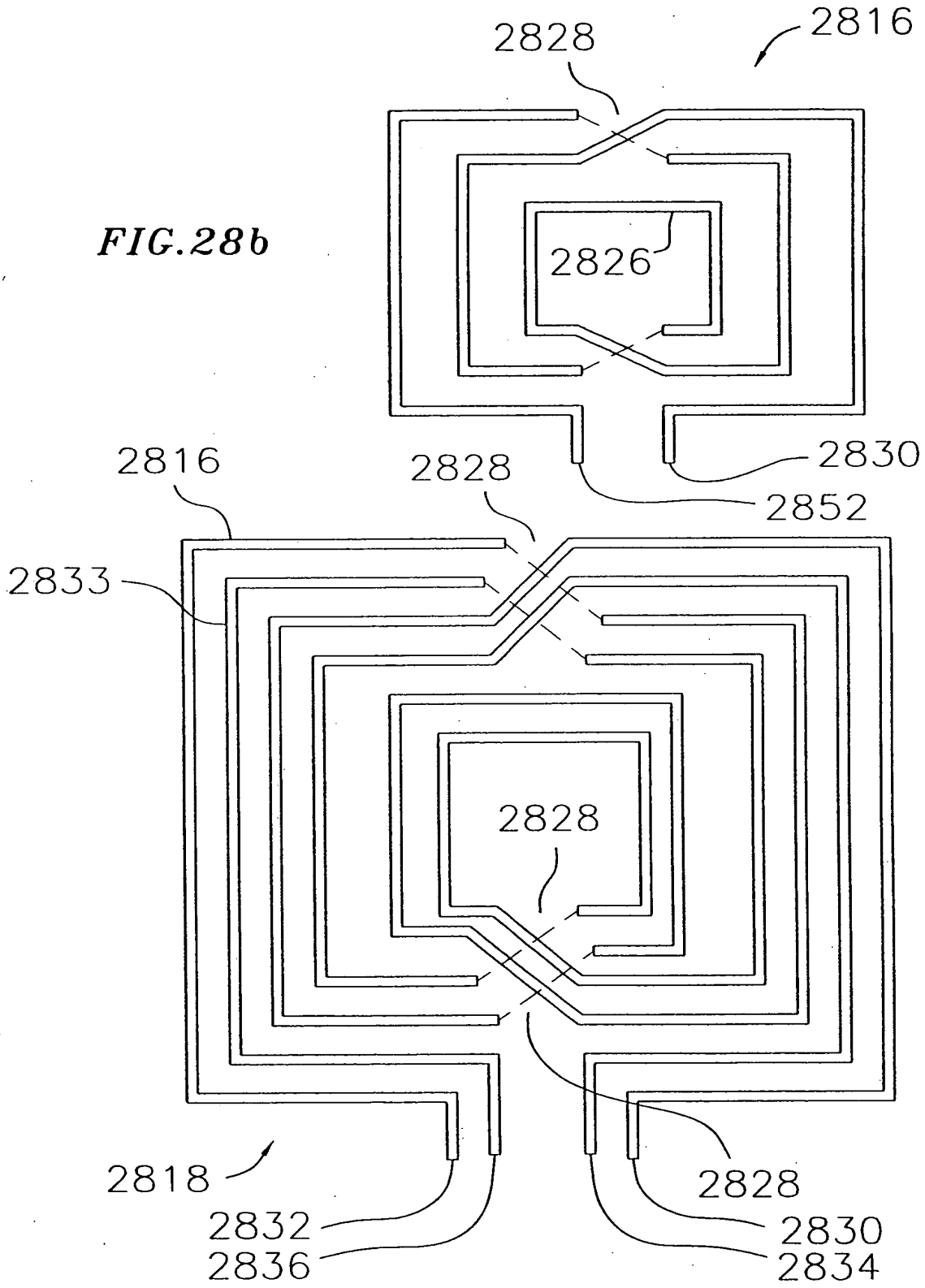
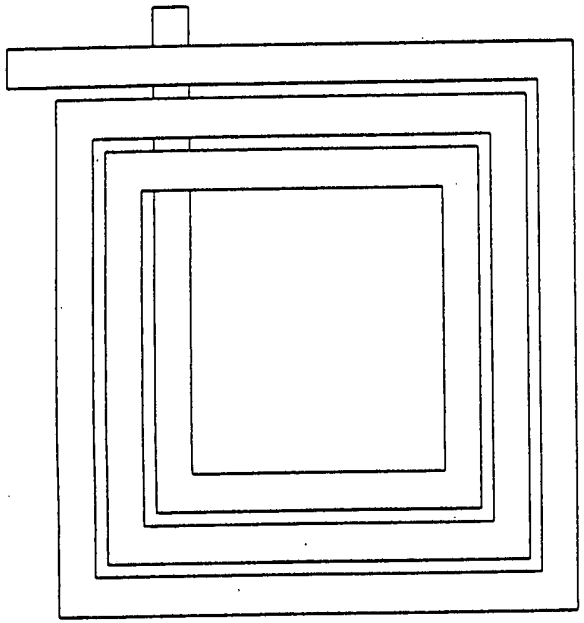
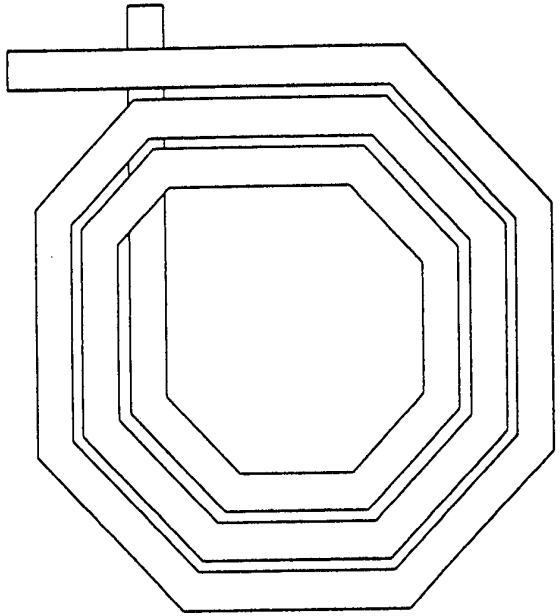

2828
2816
2826
2830
2816
2828
2852
2833
2828
2818
2828
2832
2830
2836
2834

FIG.28c



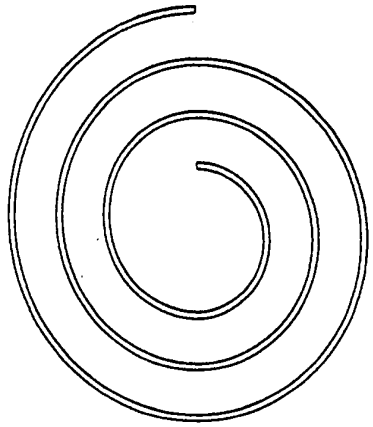
2820

FIG.28d



2822

FIG.28e



2824

FIG.28f

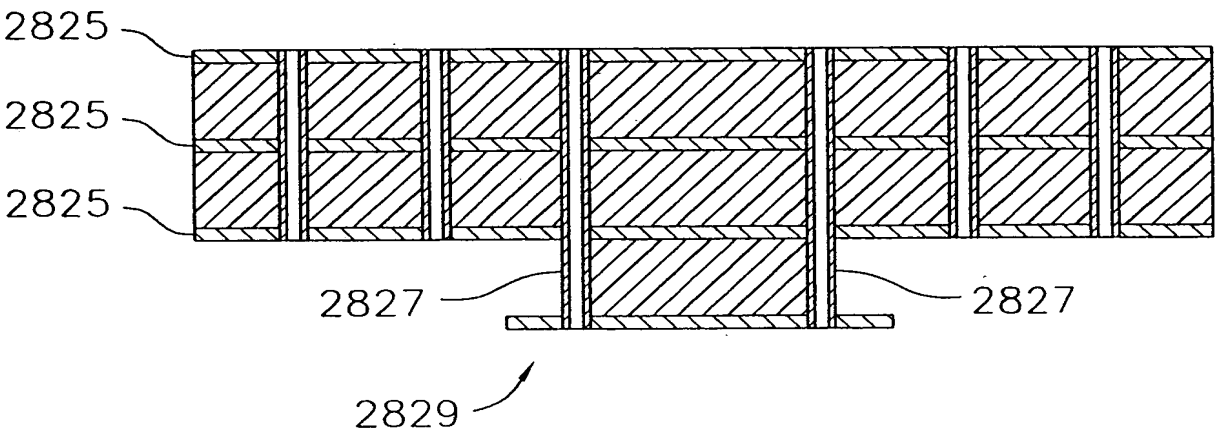


FIG.28g

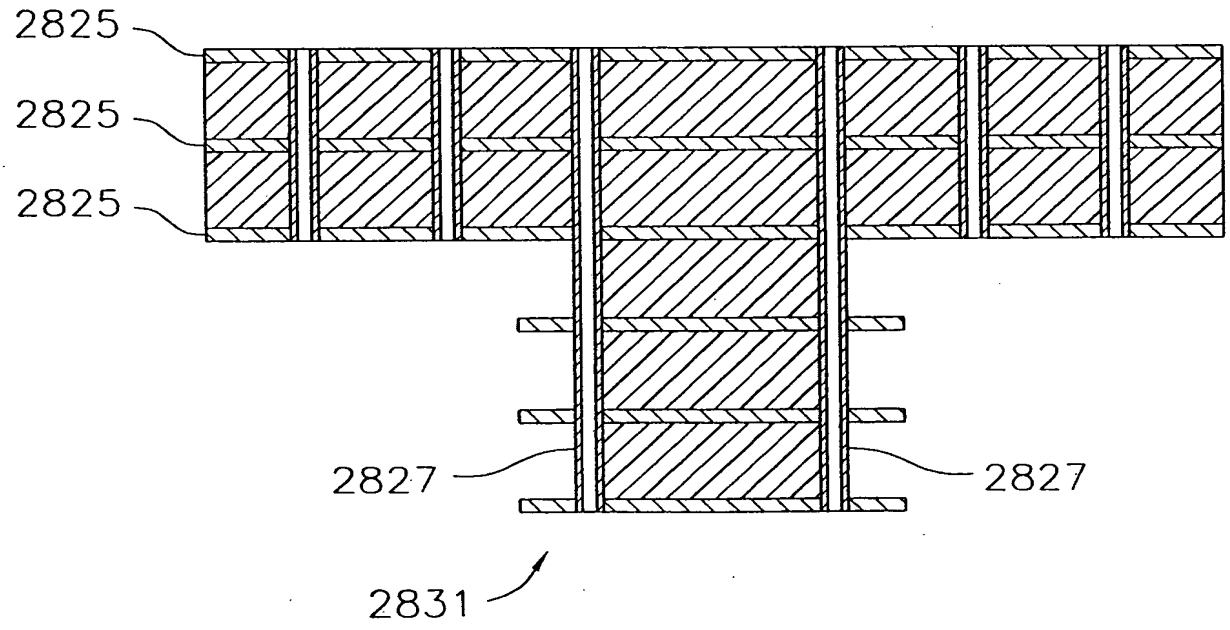


FIG.28h

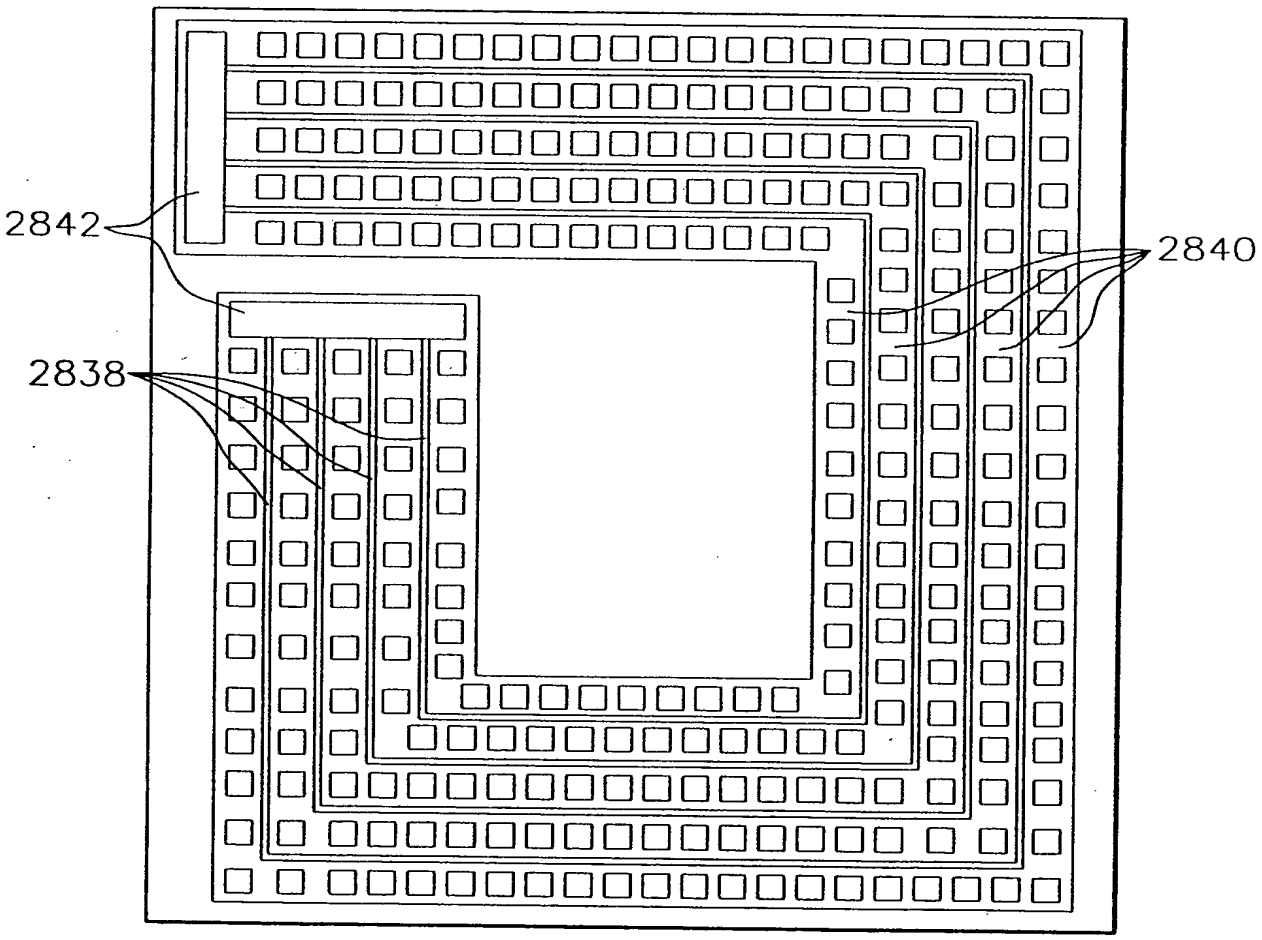


FIG.28i

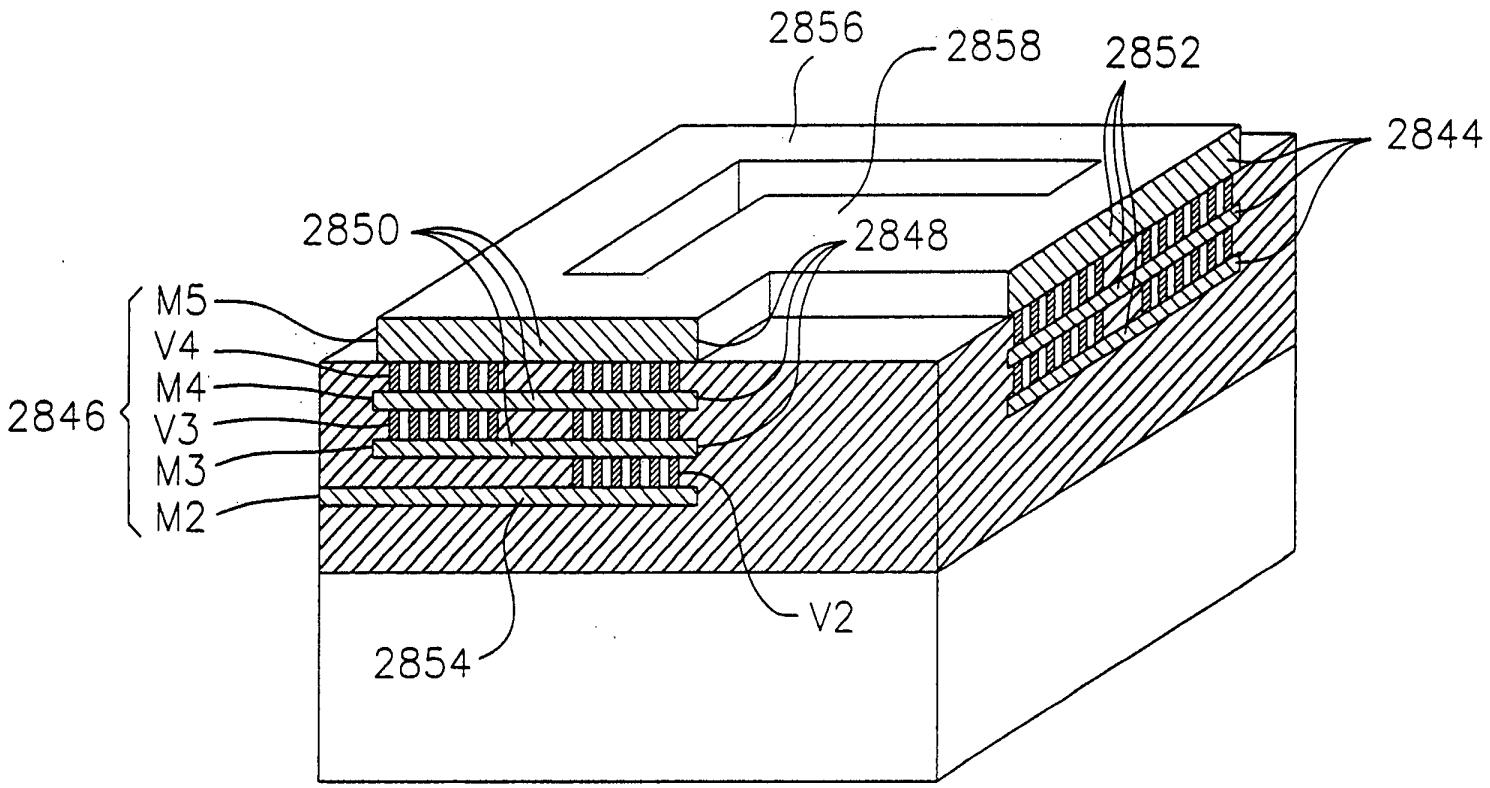


FIG. 28j

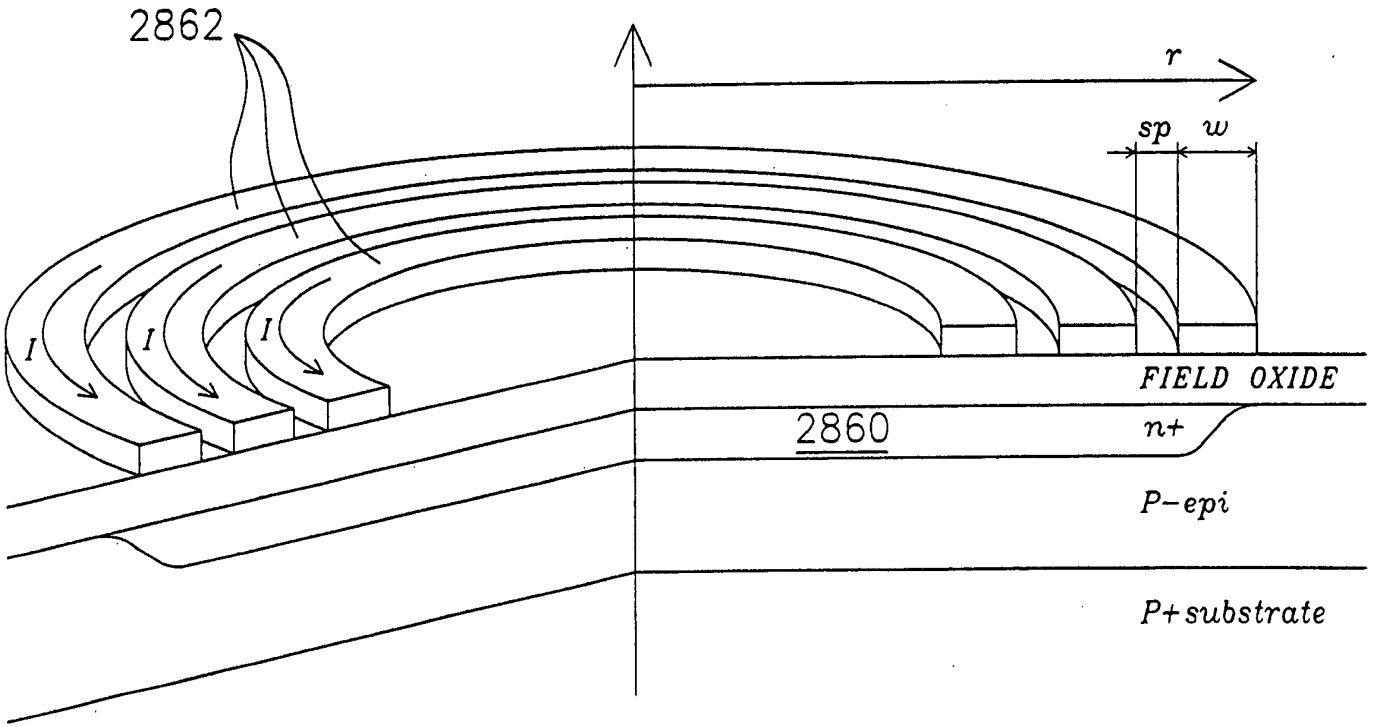


FIG.28k

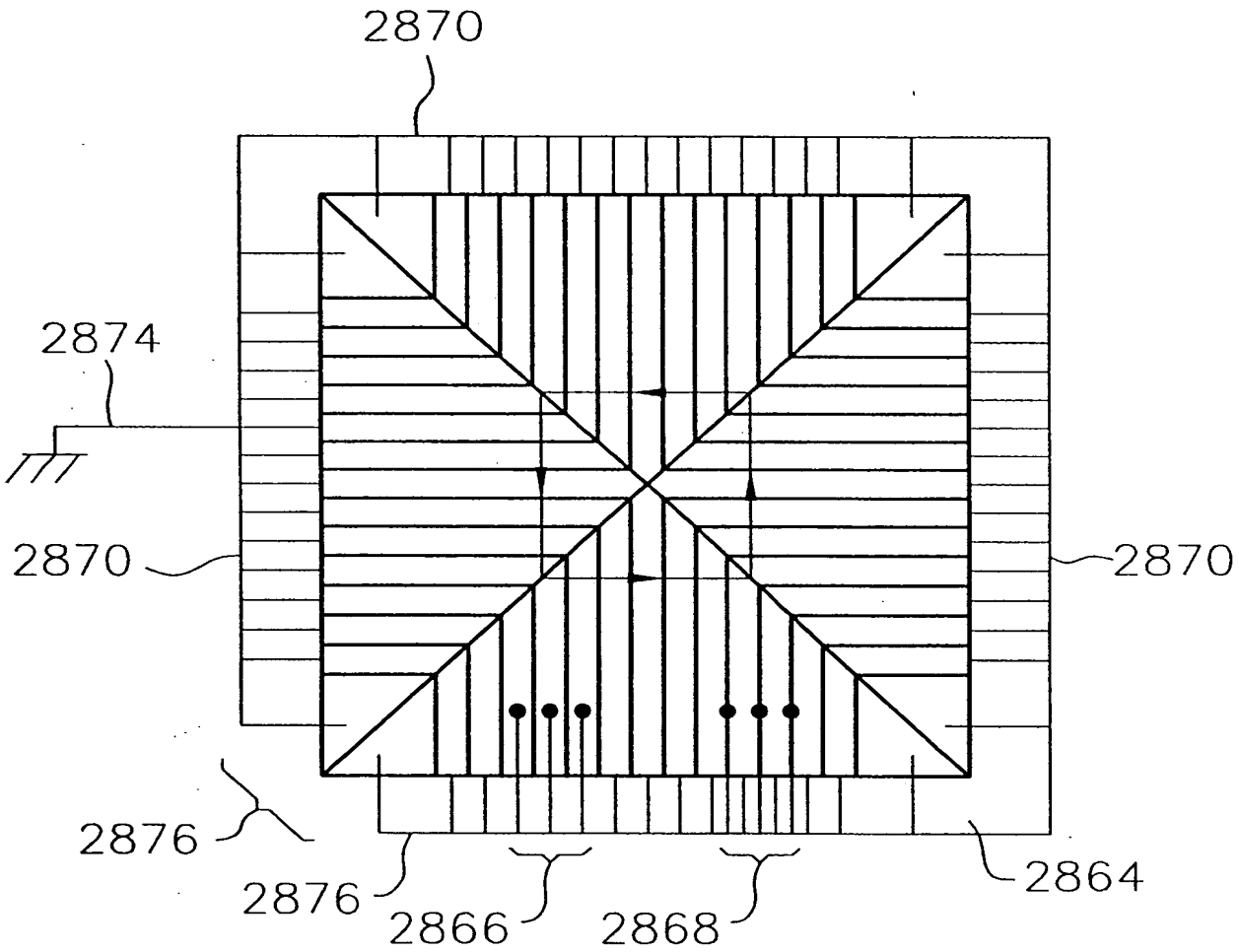


FIG.29

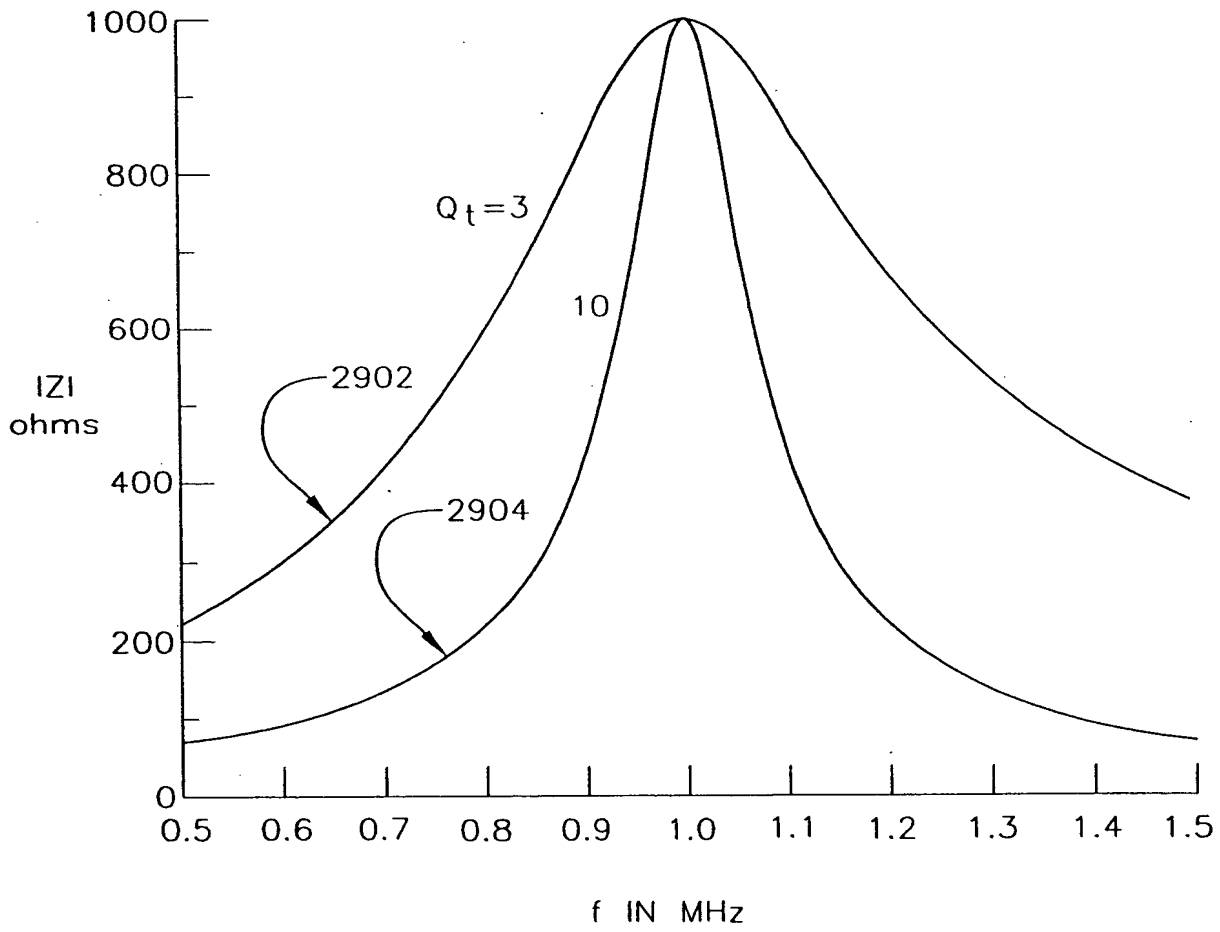

1000
800
600
400
200
0
|Z|
ohms
$Q_t=3$
10
2902
2904
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
f IN MHz

FIG.30

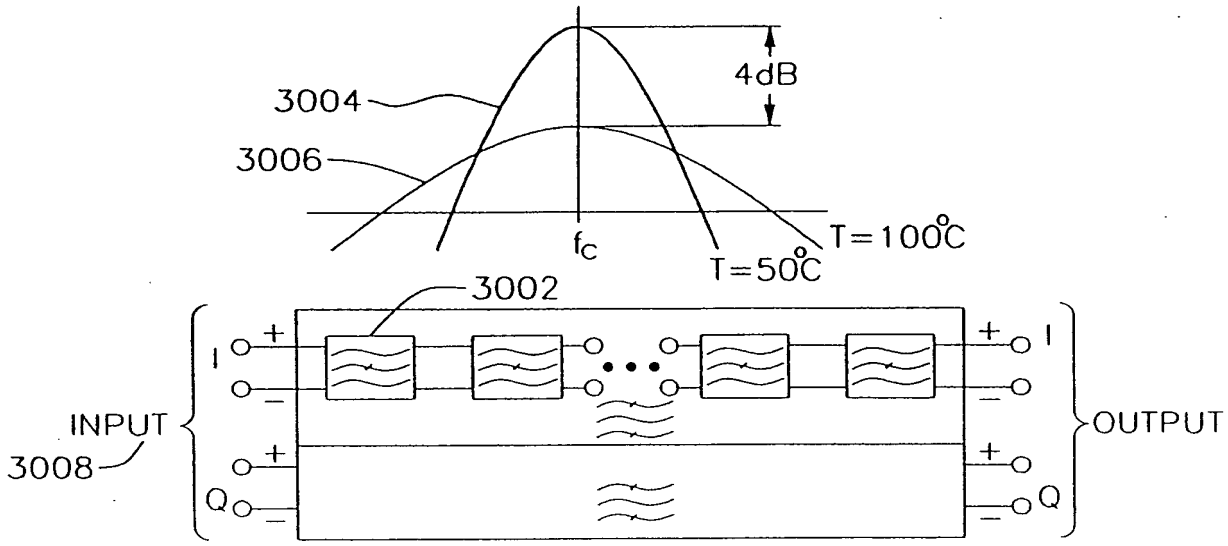


FIG.31A

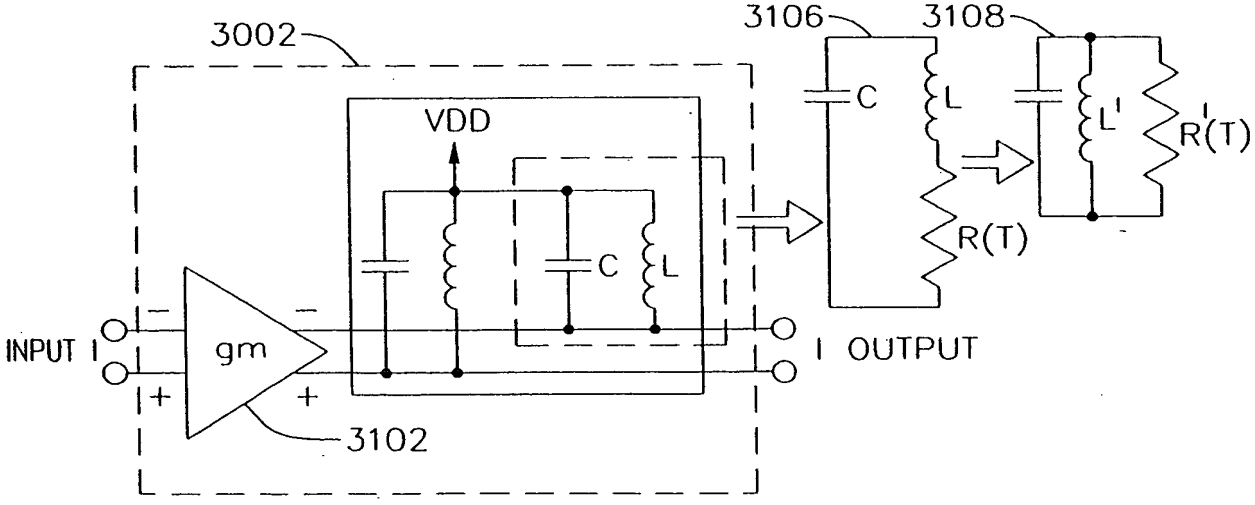


FIG. 31B

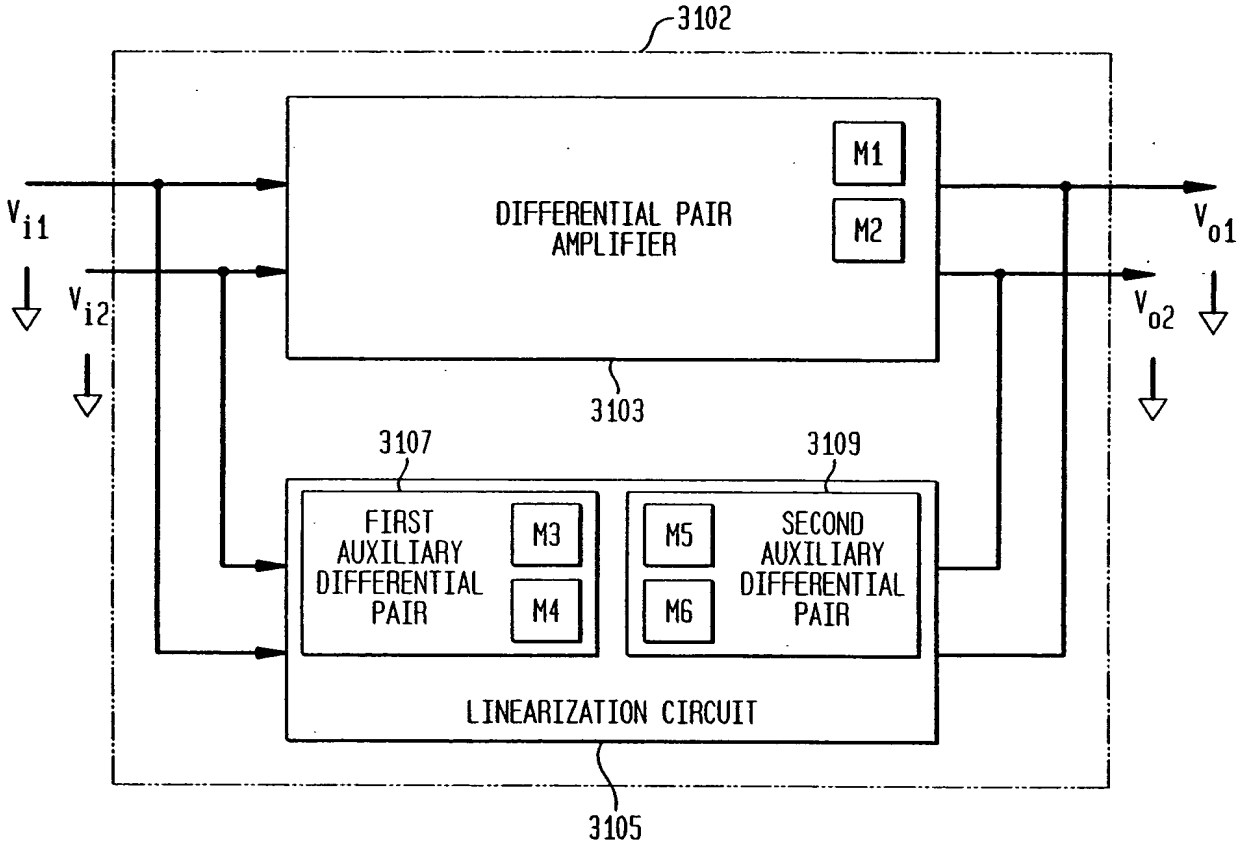

3102
M1
M2
DIFFERENTIAL PAIR AMPLIFIER
V_{i1}
V_{i2}
V_{o1}
V_{o2}
3103
3107
3109
FIRST AUXILIARY DIFFERENTIAL PAIR
M3
M4
M5
M6
SECOND AUXILIARY DIFFERENTIAL PAIR
LINEARIZATION CIRCUIT
3105

FIG. 31C

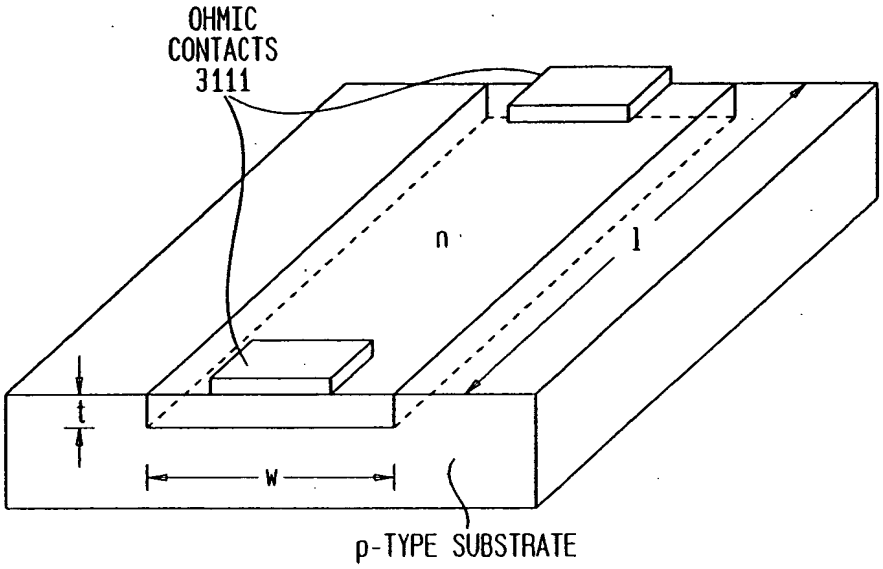


FIG. 31D

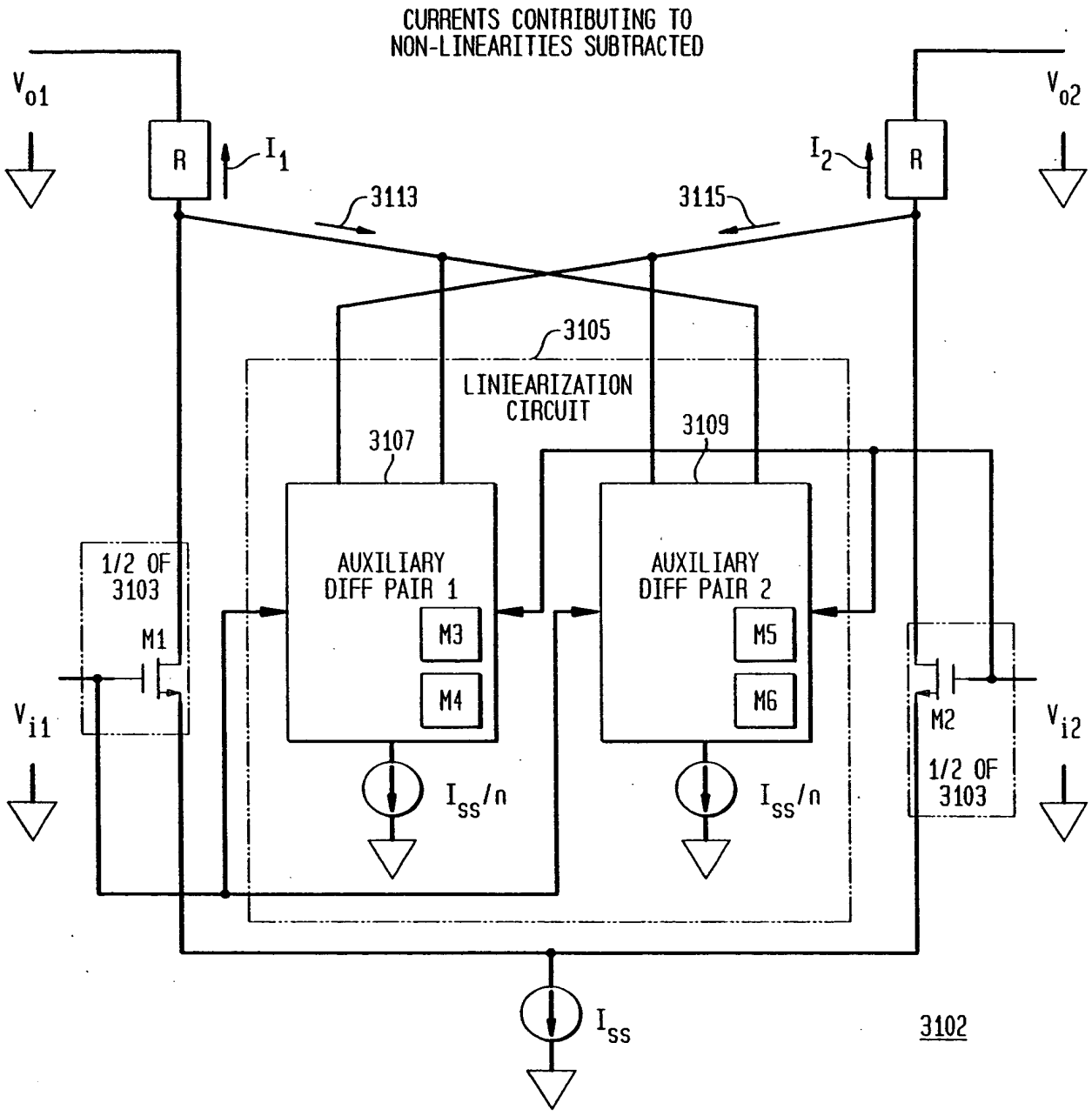

CURRENTS CONTRIBUTING TO
NON-LINEARITIES SUBTRACTED
V_{o1}
V_{o2}
R
I_1
I_2
R
3113
3115
3105
LINIEARIZATION
CIRCUIT
3107
3109
1/2 OF
3103
AUXILIARY
DIFF PAIR 1
AUXILIARY
DIFF PAIR 2
M1
M3
M4
M5
M6
M2
V_{i1}
V_{i2}
I_{ss}/n
I_{ss}/n
1/2 OF
3103
I_{ss}
3102

FIG. 31E

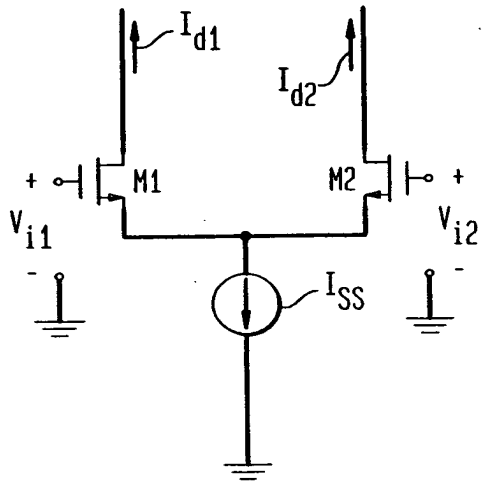


FIG. 31F

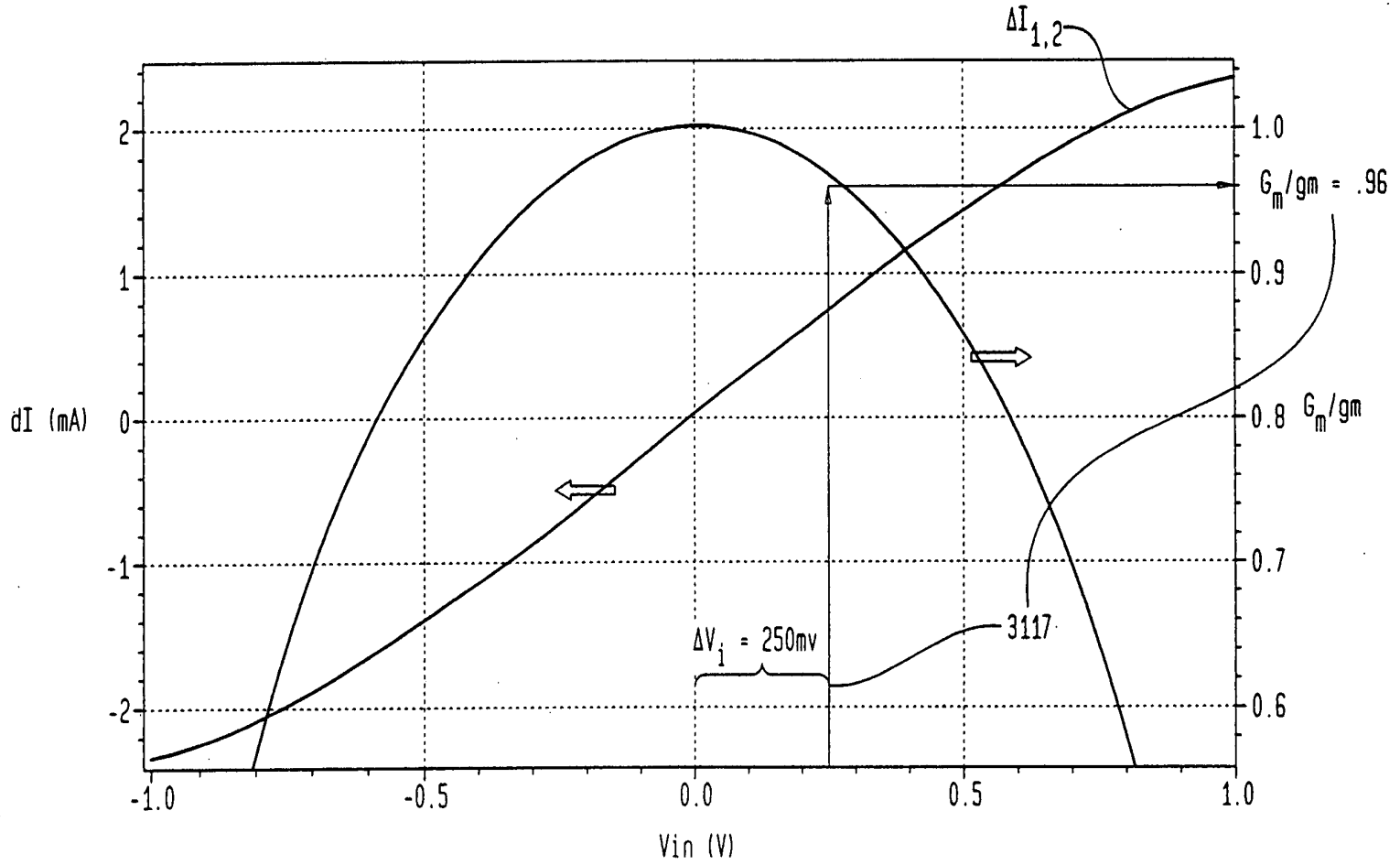

ΔI1,2
Gm/gm = .96
Gm/gm
dI (mA)
2
1
0
-1
-2
1.0
0.9
0.8
0.7
0.6
ΔVi = 250mv
3117
-1.0
-0.5
0.0
0.5
1.0
Vin (V)

FIG. 31G

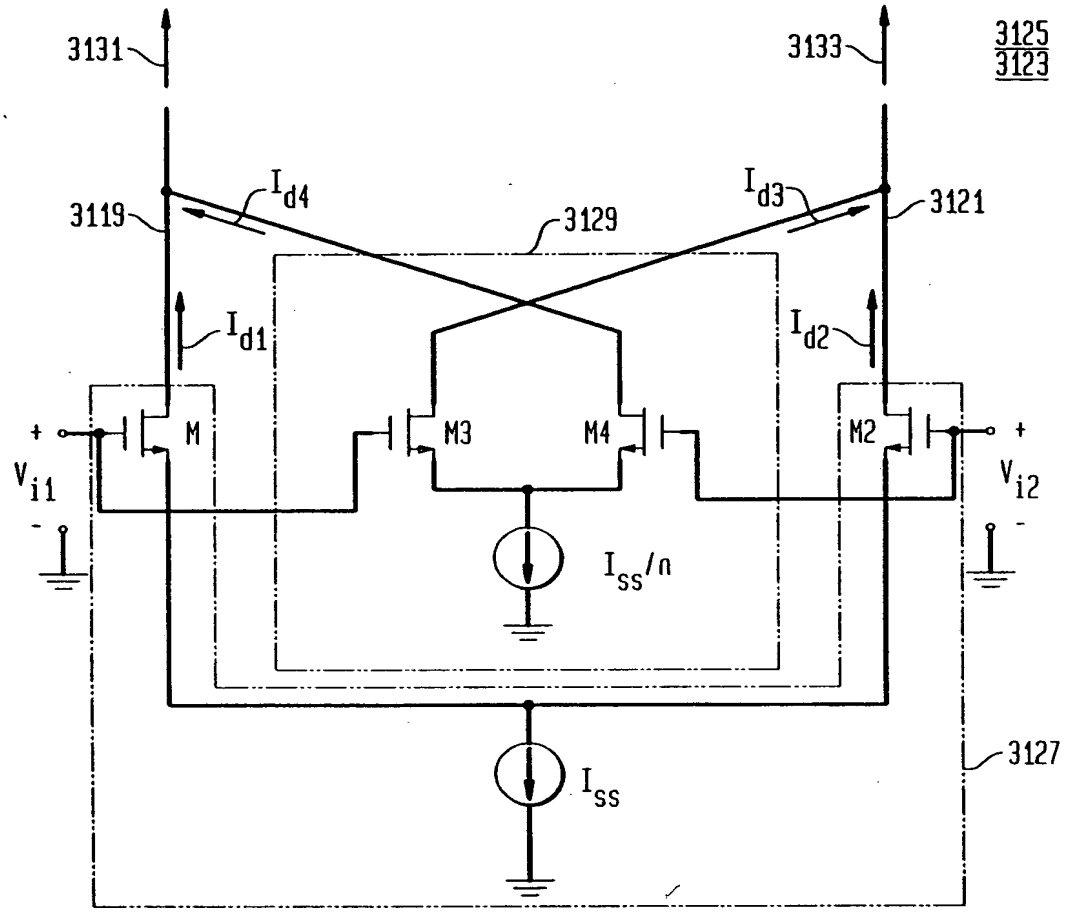

3131
3133
3125
3123
3119
I_{d4}
I_{d3}
3121
3129
I_{d1}
I_{d2}
M
M3
M4
M2
+
V_{i1}
-
+
V_{i2}
-
I_{ss}/n
I_{ss}
3127

FIG. 31H

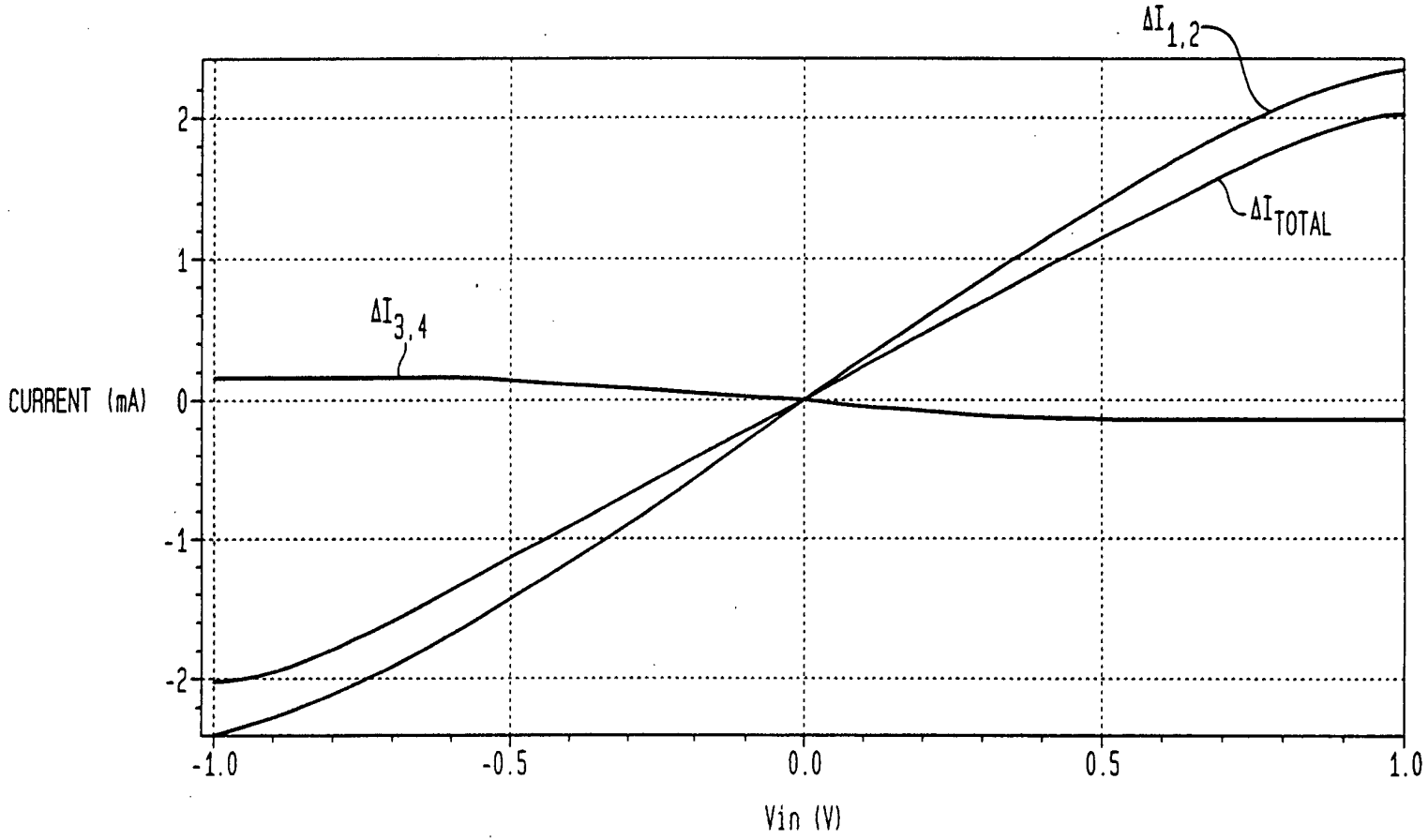


FIG. 31I

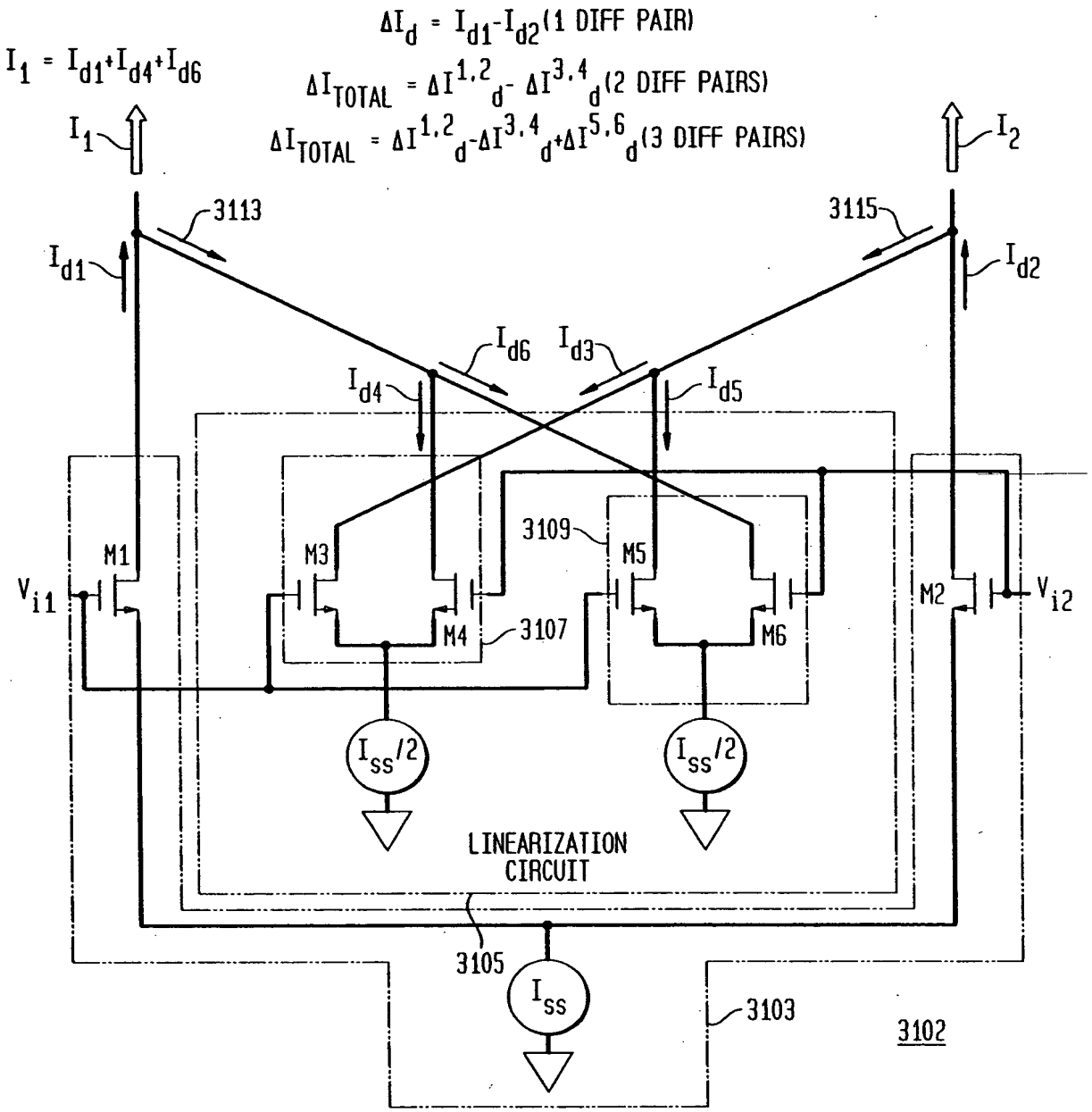

$\Delta I_d = I_{d1} - I_{d2}$ (1 DIFF PAIR)
$I_1 = I_{d1} + I_{d4} + I_{d6}$
$\Delta I_{TOTAL} = \Delta I^{1,2}{}_d - \Delta I^{3,4}{}_d$ (2 DIFF PAIRS)
$\Delta I_{TOTAL} = \Delta I^{1,2}{}_d - \Delta I^{3,4}{}_d + \Delta I^{5,6}{}_d$ (3 DIFF PAIRS)
I_1
I_2
3113
3115
I_{d1}
I_{d2}
I_{d6}
I_{d3}
I_{d4}
I_{d5}
3109
M1
M3
M5
M2
V_{i1}
V_{i2}
M4
3107
M6
$I_{ss}/2$
$I_{ss}/2$
LINEARIZATION CIRCUIT
3105
I_{ss}
3103
3102

FIG. 31J

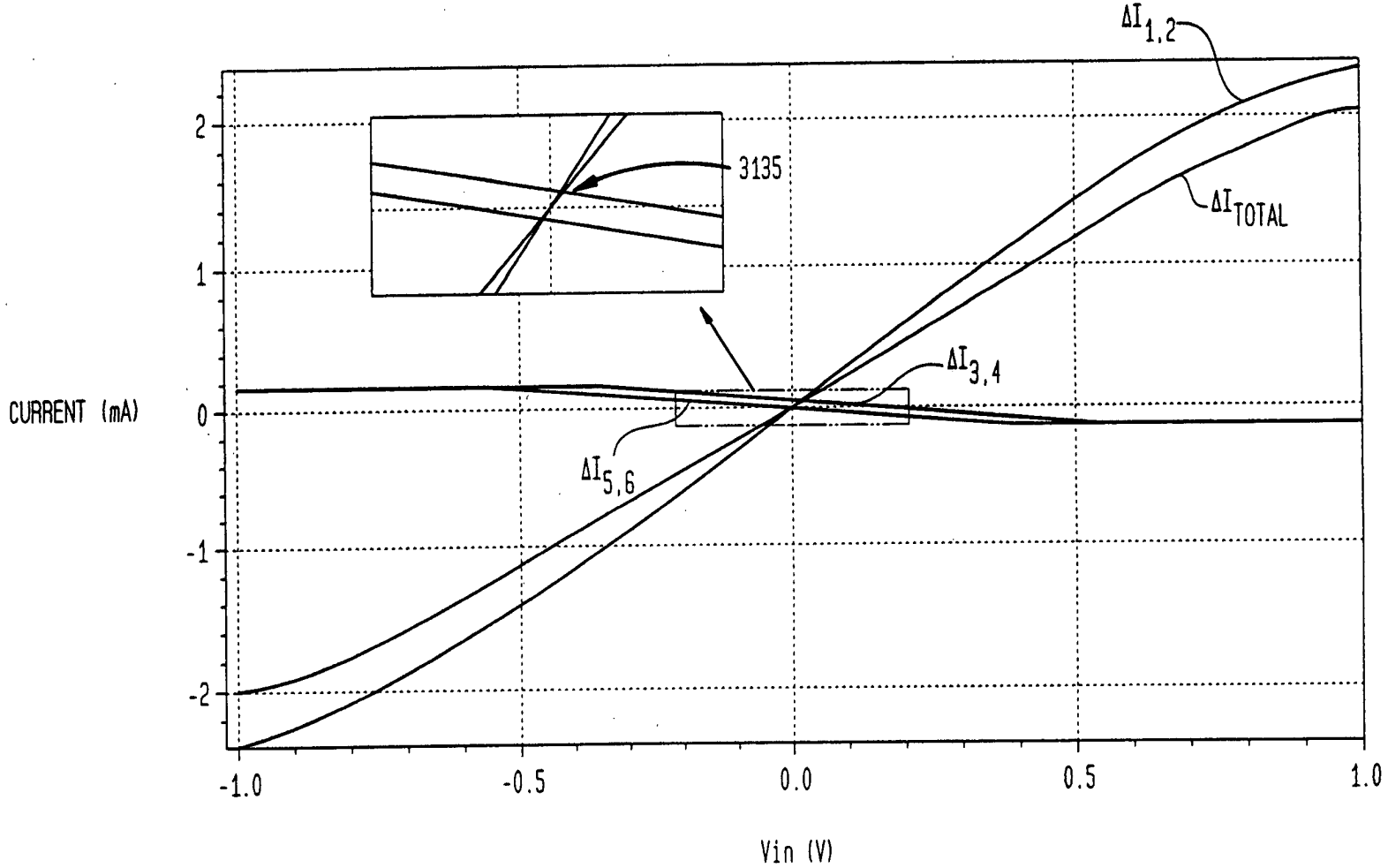

$\Delta I_{1,2}$
ΔI_{TOTAL}
$\Delta I_{3,4}$
$\Delta I_{5,6}$
3135
CURRENT (mA)
2
1
0
-1
-2
-1.0
-0.5
0.0
0.5
1.0
Vin (V)

FIG. 31K

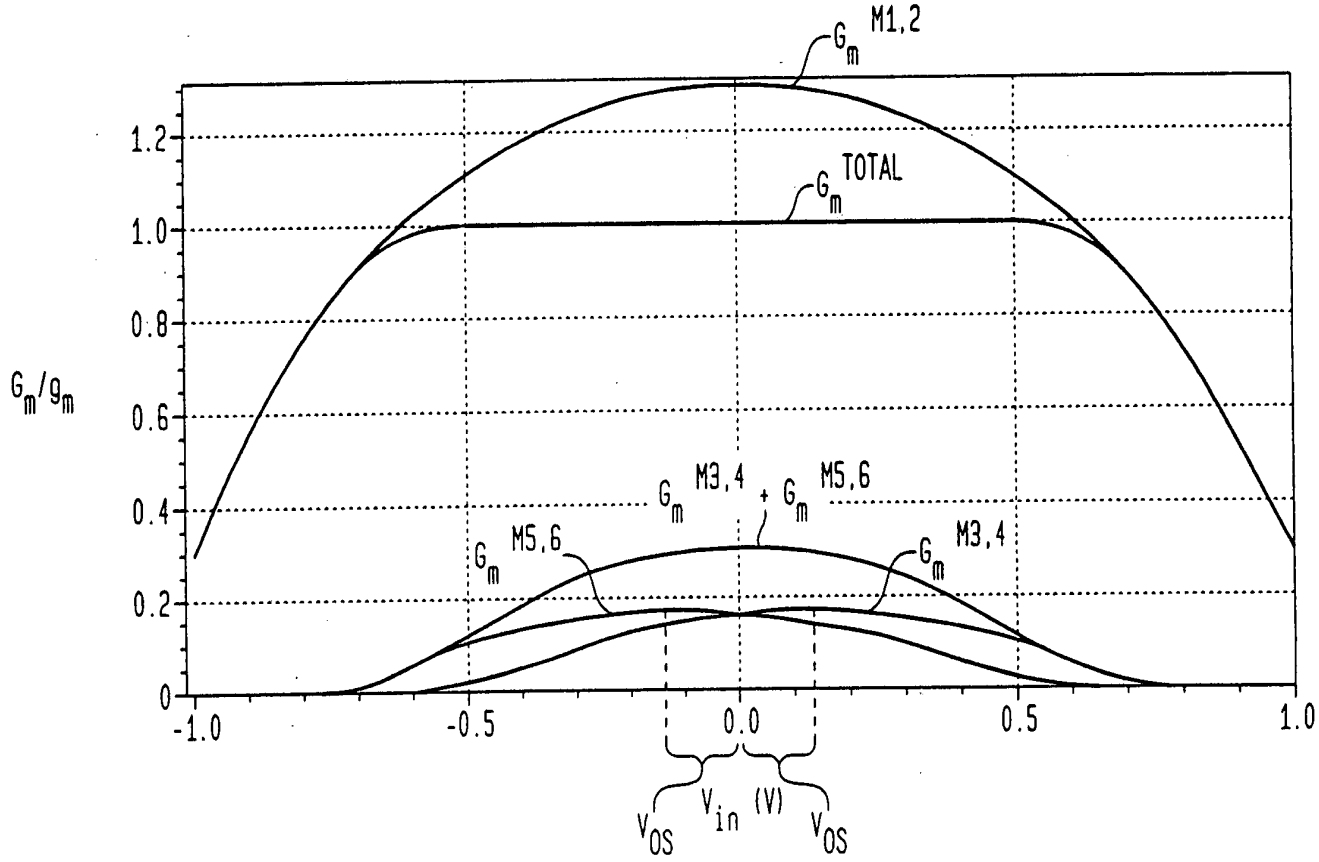

G_m M1,2
G_m TOTAL
G_m M3,4 + G_m M5,6
G_m M5,6
G_m M3,4
G_m/g_m
1.2
1.0
0.8
0.6
0.4
0.2
0
-1.0
-0.5
0.0
0.5
1.0
V_{OS}
V_{in} (V)
V_{OS}

FIG. 31L

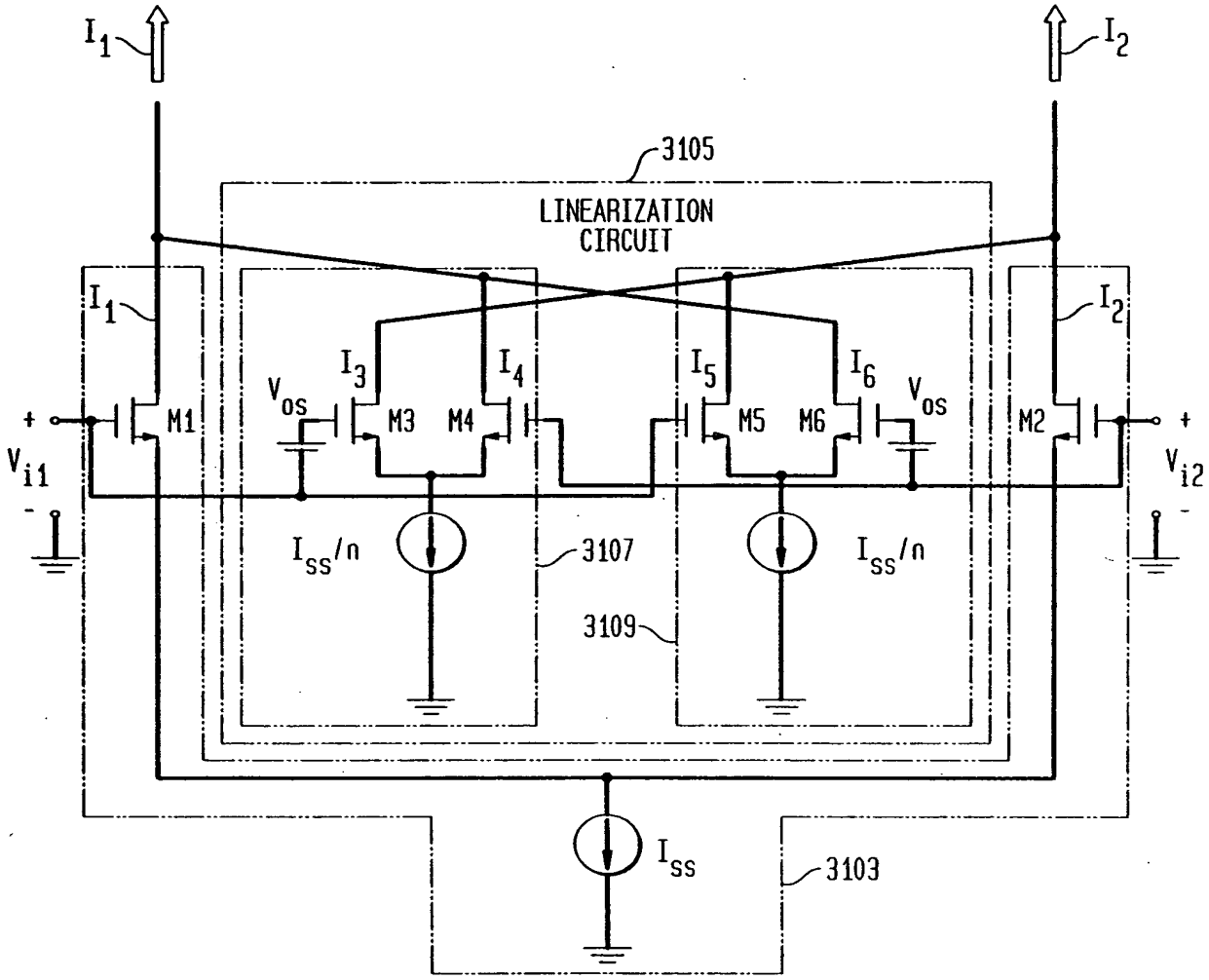

I1
I2
3105
LINEARIZATION CIRCUIT
I1
I2
I3
I4
I5
I6
Vos
Vos
M1
M3
M4
M5
M6
M2
Vi1
Vi2
Iss/n
Iss/n
3107
3109
Iss
3103

FIG. 31M

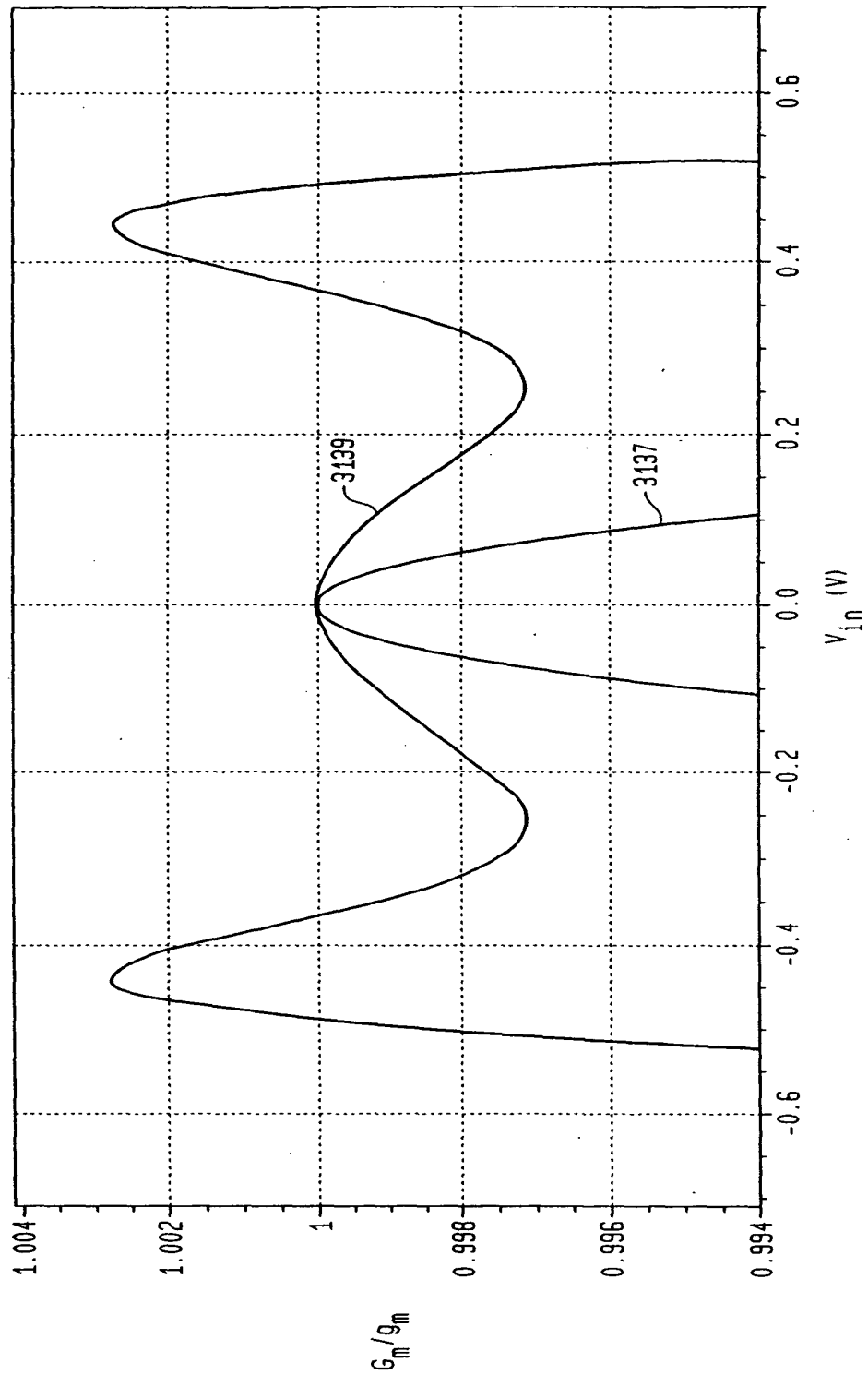

1.004
1.002
1
0.998
0.996
0.994
G_m/g_m
-0.6
-0.4
-0.2
0.0
0.2
0.4
0.6
V_{in} (V)
3139
3137

FIG. 32

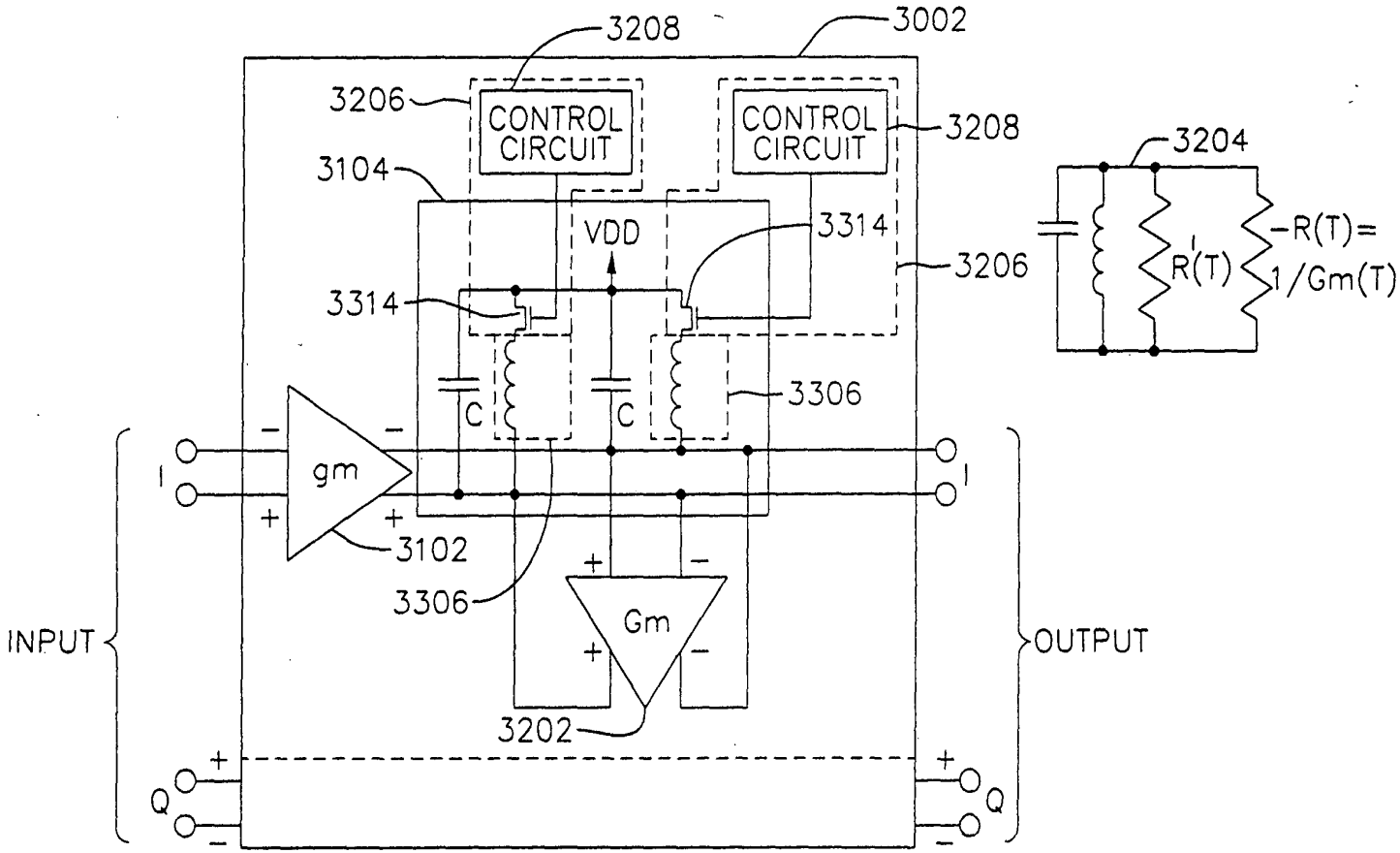

3208
3002
3206
CONTROL CIRCUIT
CONTROL CIRCUIT
3208
3104
VDD
3314
3314
3206
C
C
3306
gm
3102
3306
Gm
3202
INPUT
OUTPUT
I
I
Q
Q
3204
R(T)
R(T)=
1/Gm(T)

FIG.33

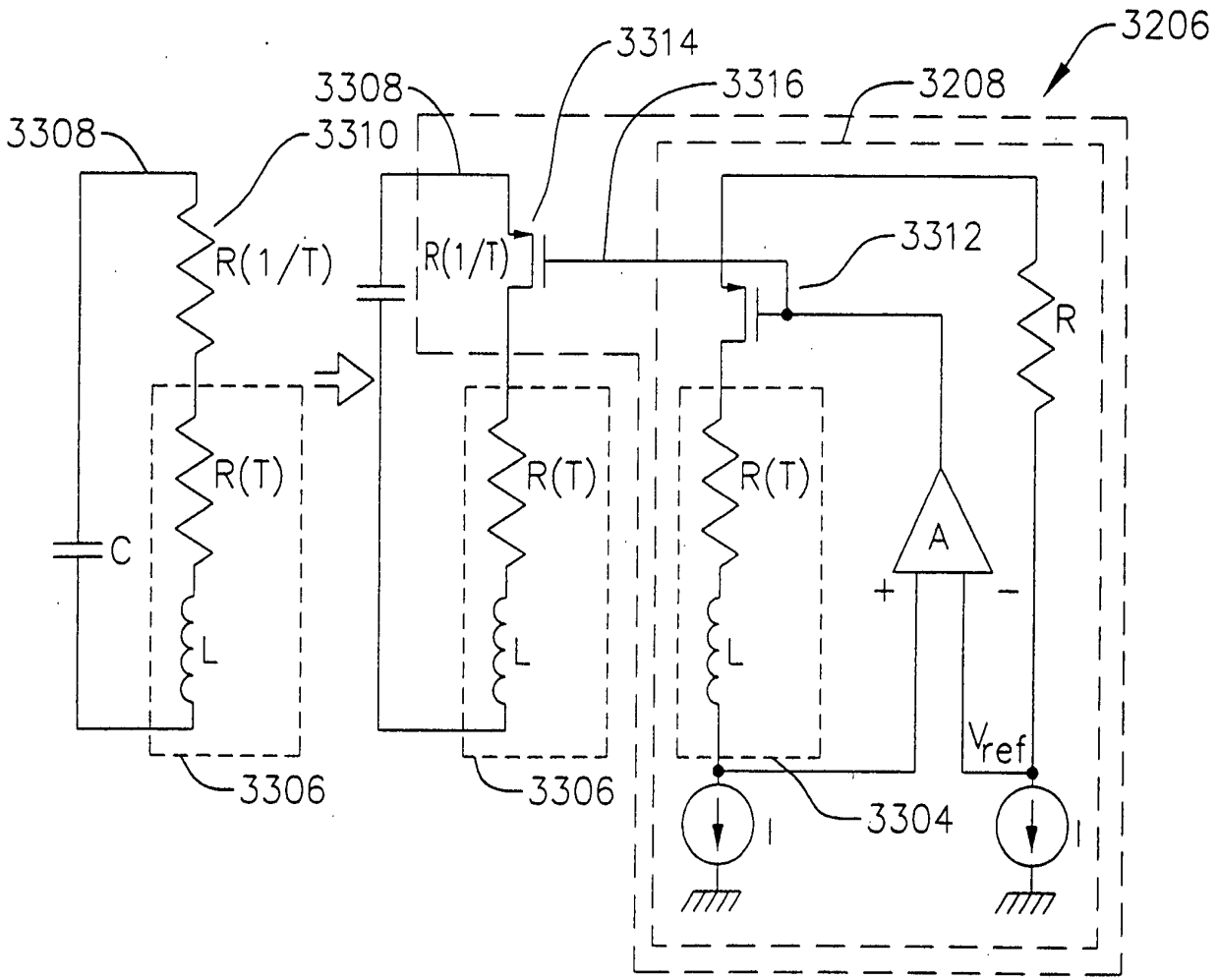

3206
3314
3308
3316
3208
3308
3310
3312
R(1/T)
R(1/T)
R
R(T)
R(T)
R(T)
C
A
+
−
L
L
L
V_{ref}
3306
3306
3304
I
I

FIG.34

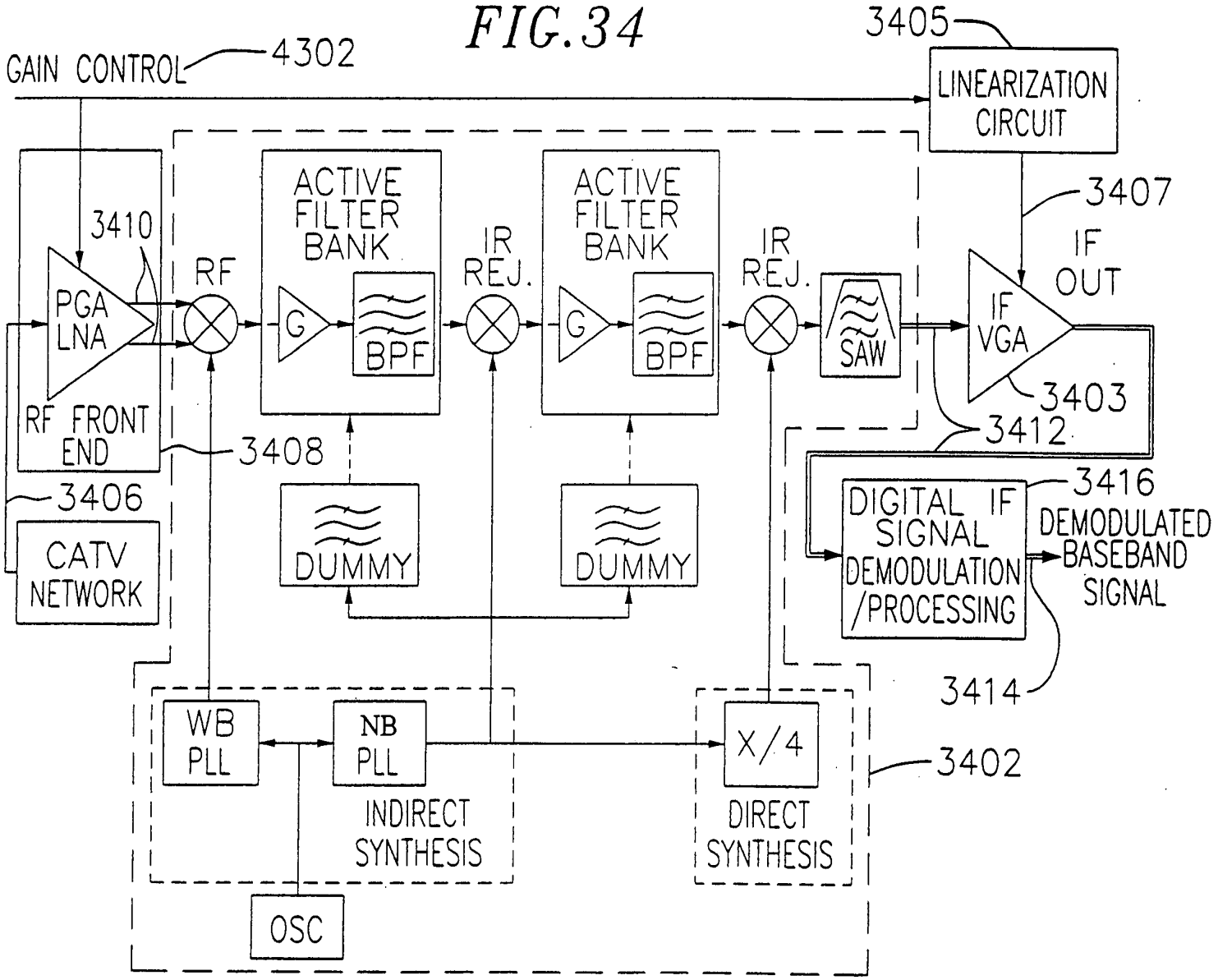

GAIN CONTROL
4302
3405
LINEARIZATION CIRCUIT
3407
IF OUT
3410
PGA LNA
RF
ACTIVE FILTER BANK
G
BPF
IR REJ.
ACTIVE FILTER BANK
G
BPF
IR REJ.
SAW
IF VGA
3403
3412
RF FRONT END
3408
3406
CATV NETWORK
DUMMY
DUMMY
3416
DIGITAL IF SIGNAL DEMODULATION /PROCESSING
DEMODULATED BASEBAND SIGNAL
3414
WB PLL
NB PLL
INDIRECT SYNTHESIS
X/4
DIRECT SYNTHESIS
3402
OSC

FIG.35

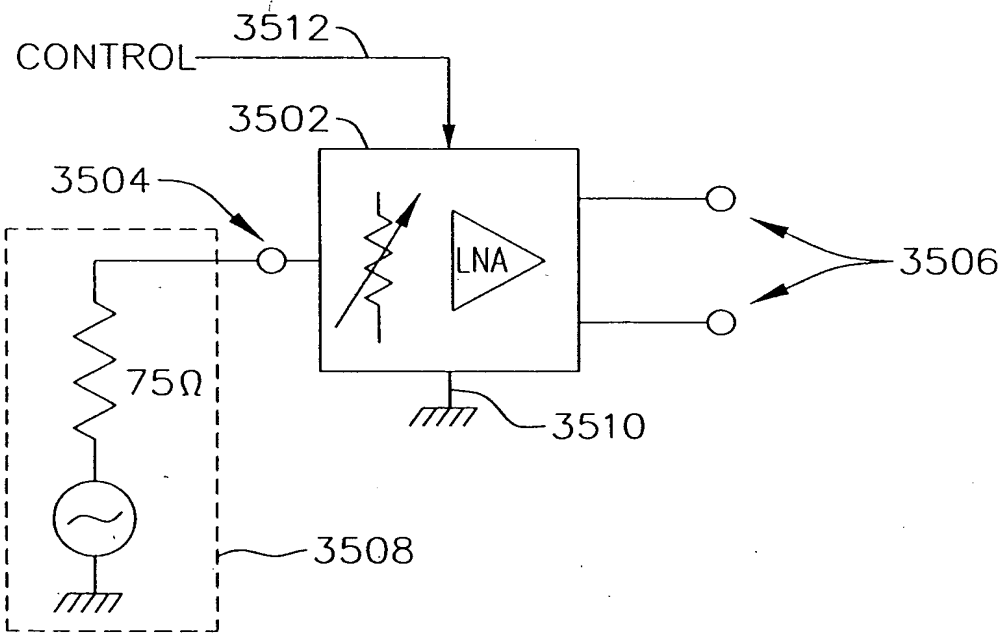


FIG.36

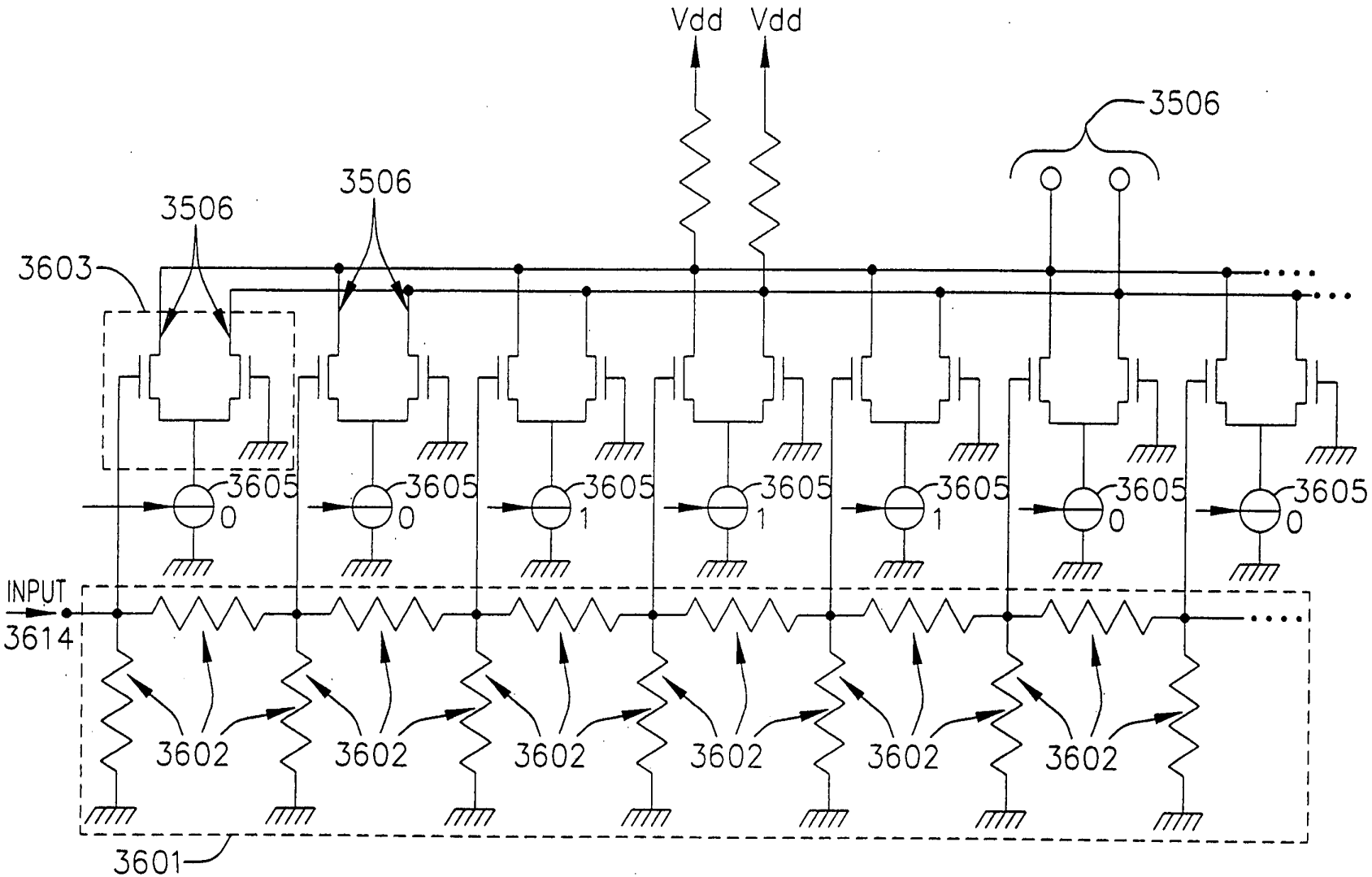

Vdd
Vdd
3506
3506
3506
3603
3605
0
3605
0
3605
1
3605
1
3605
1
3605
0
3605
0
INPUT
3614
3602
3602
3602
3602
3602
3602
3601

FIG.37

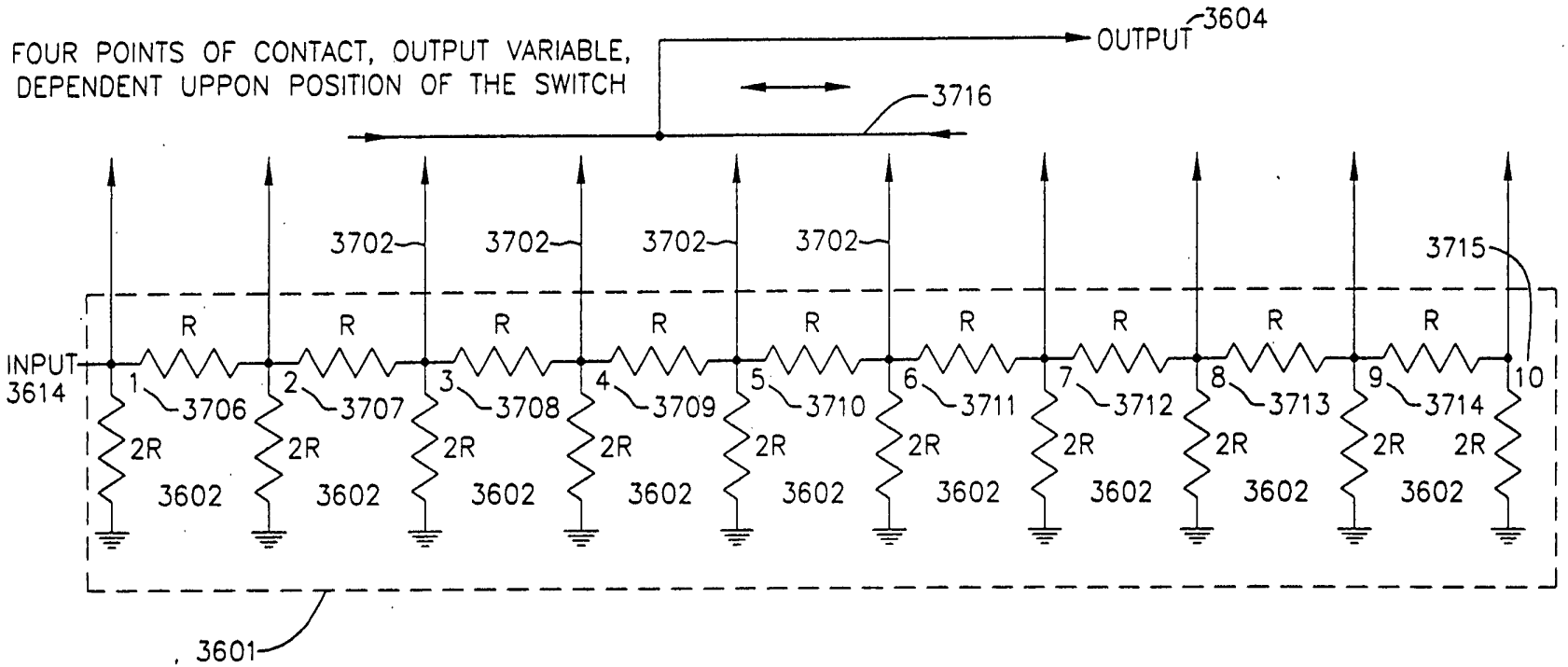

FOUR POINTS OF CONTACT, OUTPUT VARIABLE, DEPENDENT UPPON POSITION OF THE SWITCH
OUTPUT
3604
3716
3702
3702
3702
3702
3715
R
R
R
R
R
R
R
R
R
INPUT
3614
1
2
3
4
5
6
7
8
9
10
3706
3707
3708
3709
3710
3711
3712
3713
3714
2R
2R
2R
2R
2R
2R
2R
2R
2R
2R
3602
3602
3602
3602
3602
3602
3602
3602
3602
3601

FIG.38

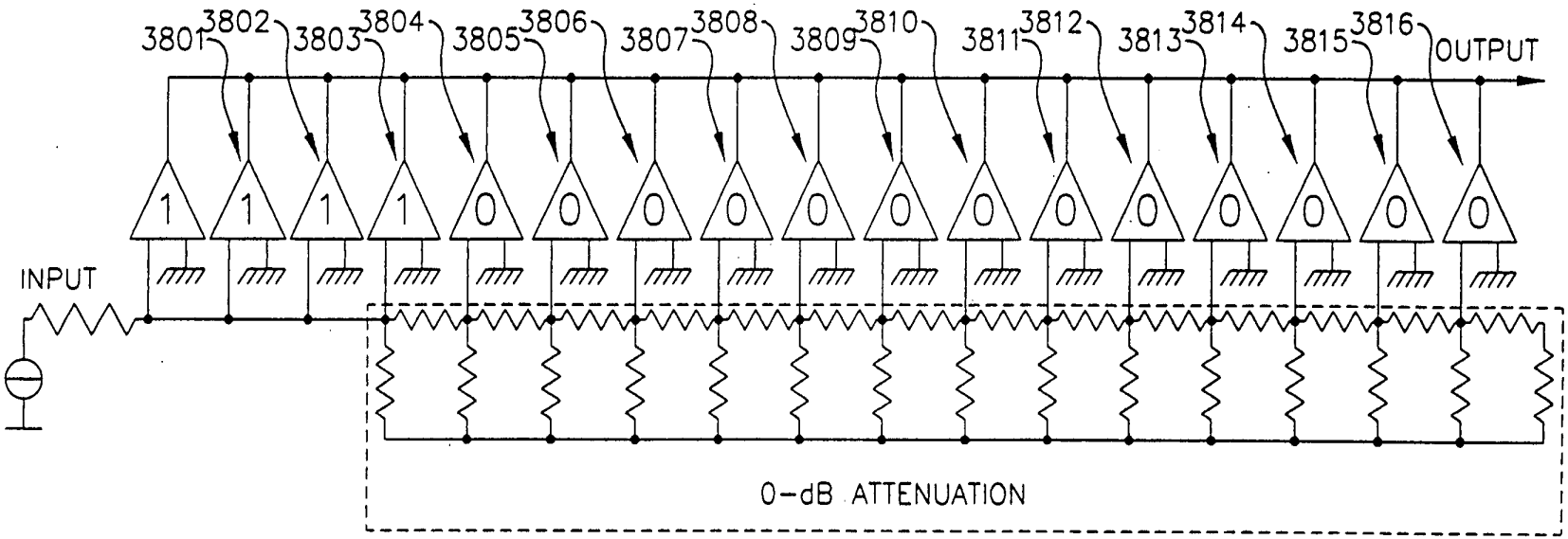

PGA SETTINGS
3801
3802
3803
3804
3805
3806
3807
3808
3809
3810
3811
3812
3813
3814
3815
3816
OUTPUT
1
1
1
1
0
0
0
0
0
0
0
0
0
0
0
0
INPUT
0-dB ATTENUATION

FIG.39

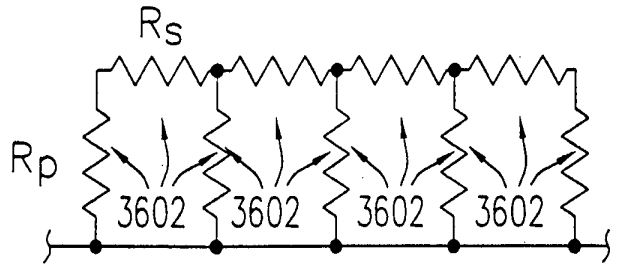

Rs
Rp
3602
3602
3602
3602

FIG.40

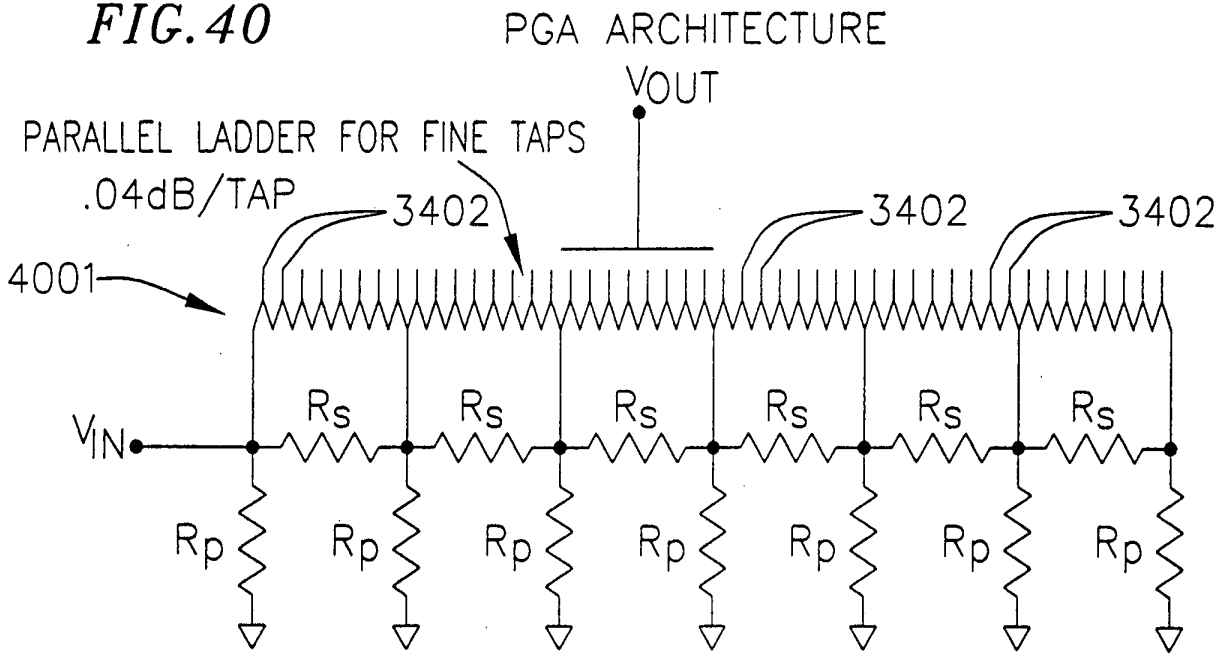

PGA ARCHITECTURE
VOUT
PARALLEL LADDER FOR FINE TAPS
.04dB/TAP
3402
3402
3402
4001
VIN
Rs
Rs
Rs
Rs
Rs
Rs
Rp
Rp
Rp
Rp
Rp
Rp
Rp

FIG.41

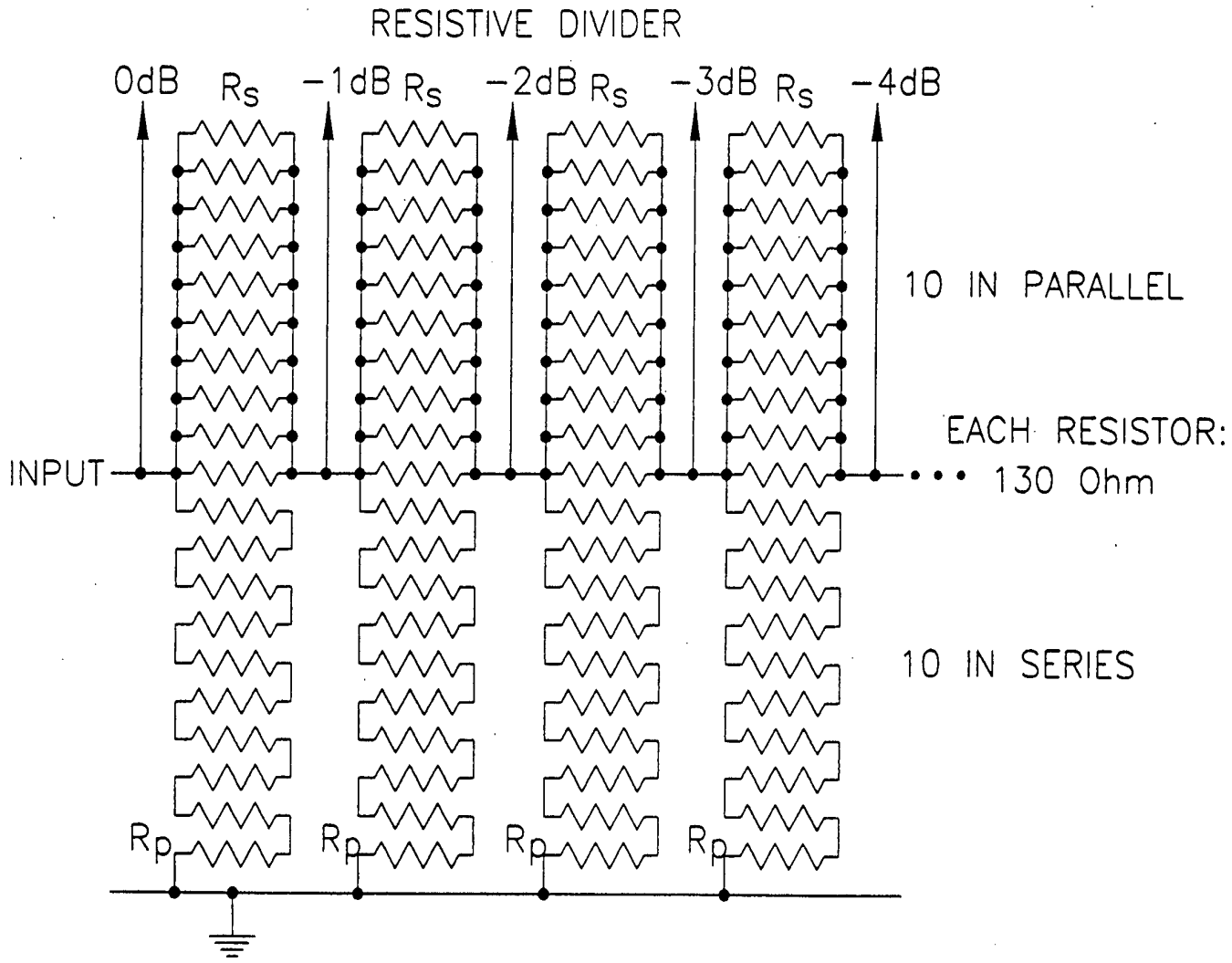

RESISTIVE DIVIDER
0dB
Rs
−1dB
Rs
−2dB
Rs
−3dB
Rs
−4dB
10 IN PARALLEL
EACH RESISTOR:
130 Ohm
INPUT
10 IN SERIES
Rp
Rp
Rp
Rp

FIG. 42

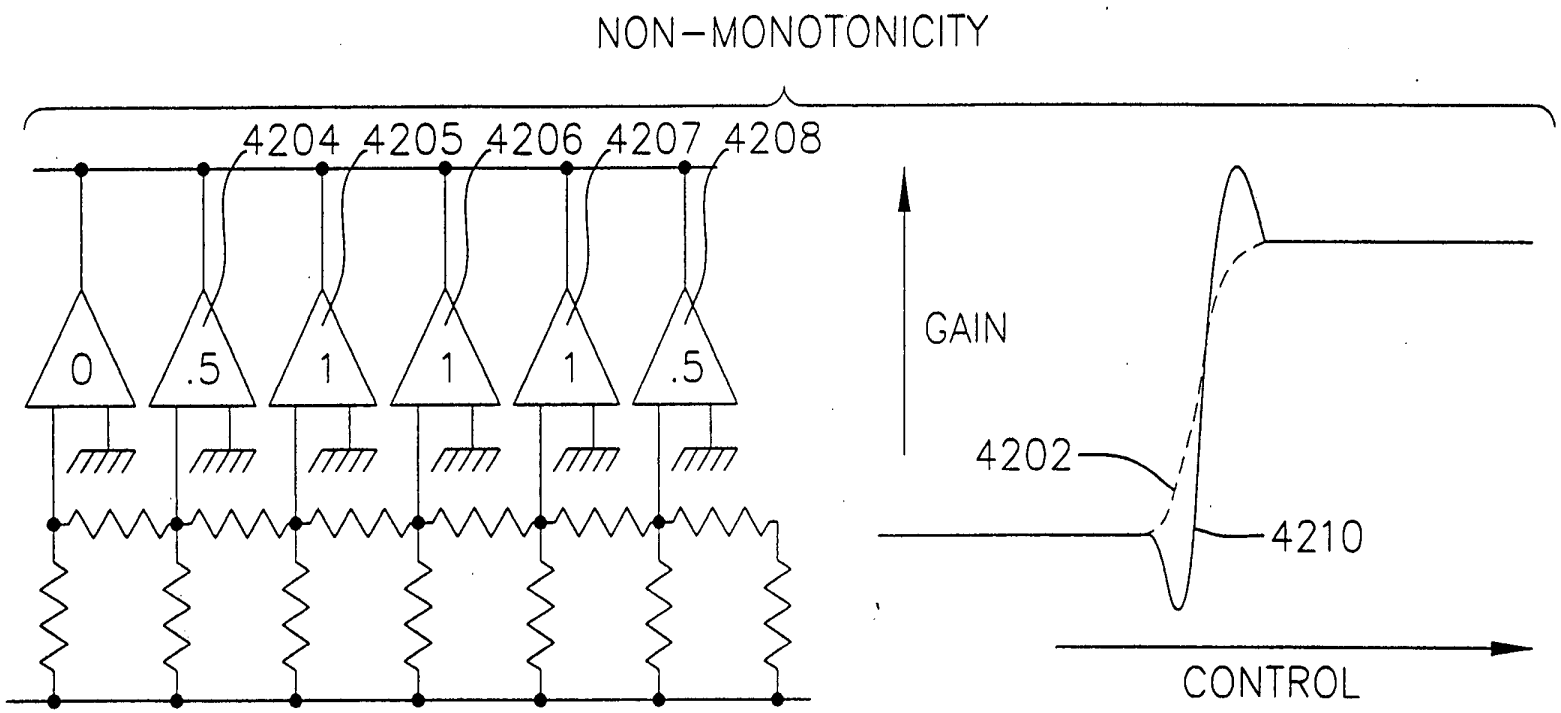

NON–MONOTONICITY
4204
4205
4206
4207
4208
0
.5
1
1
1
.5
GAIN
4202
4210
CONTROL

FIG.43

CLAMPING CONTROL RANGE.

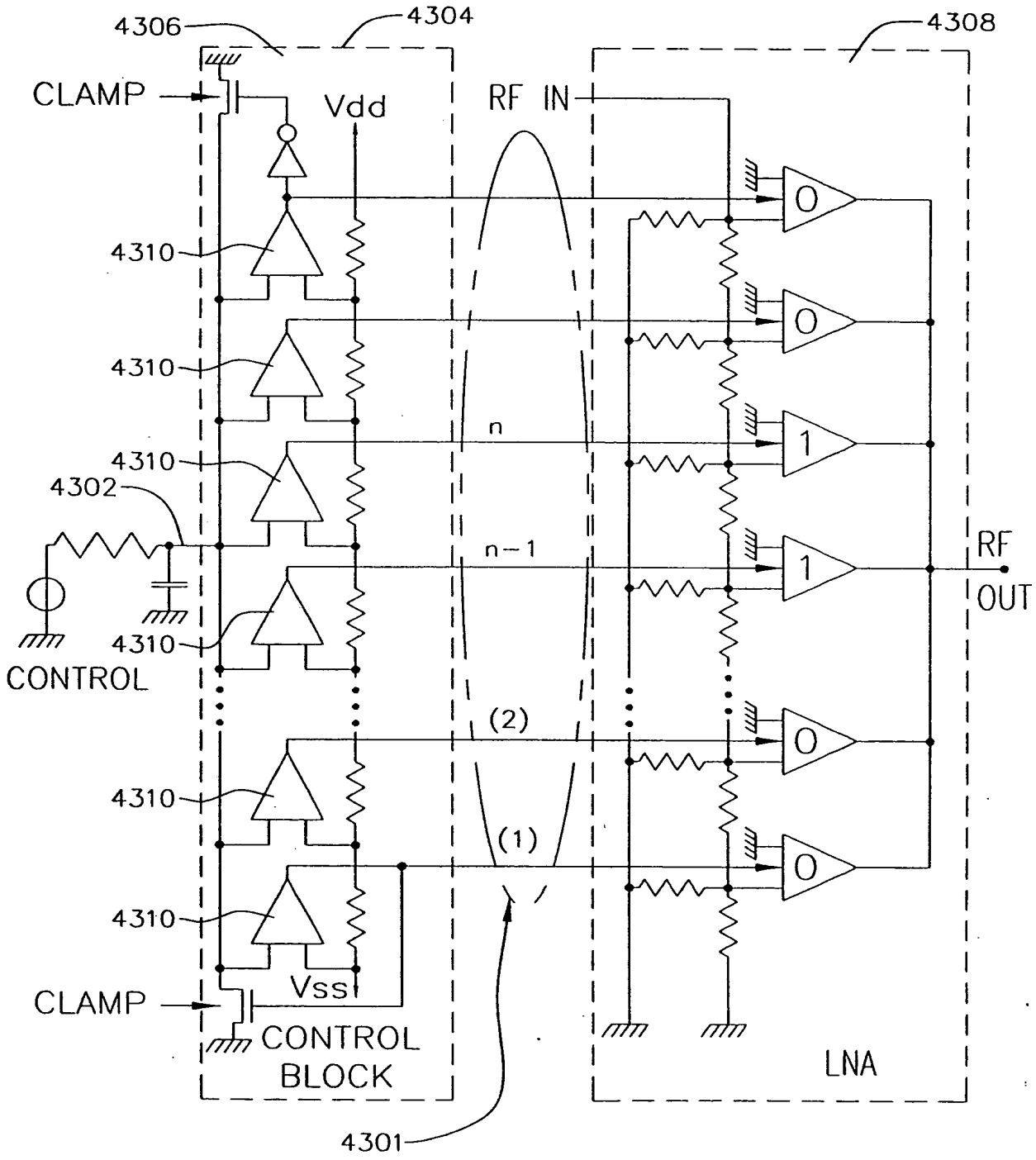


FIG. 44α

CONTROLLED GAIN COMPARATOR

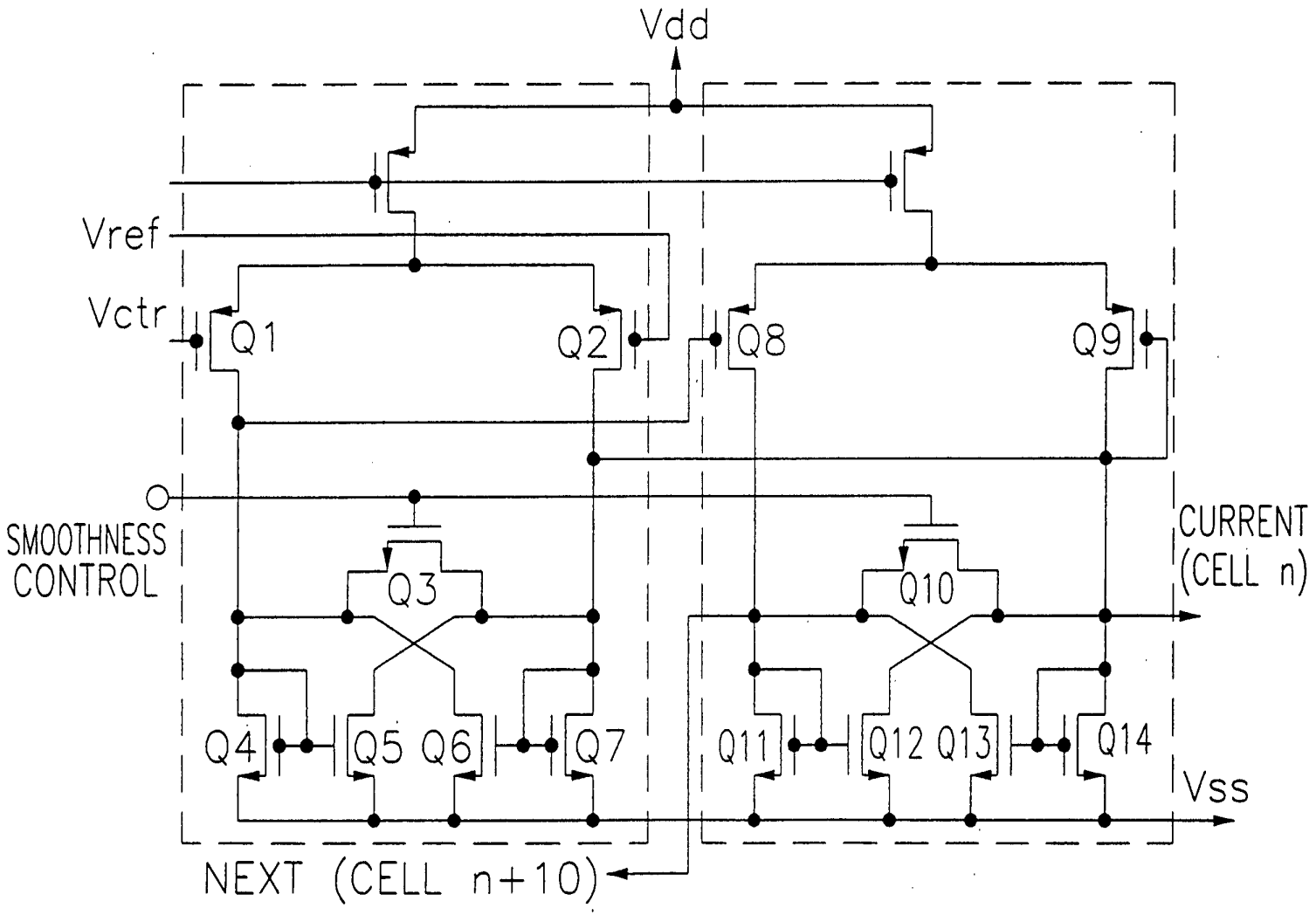


FIG.44b

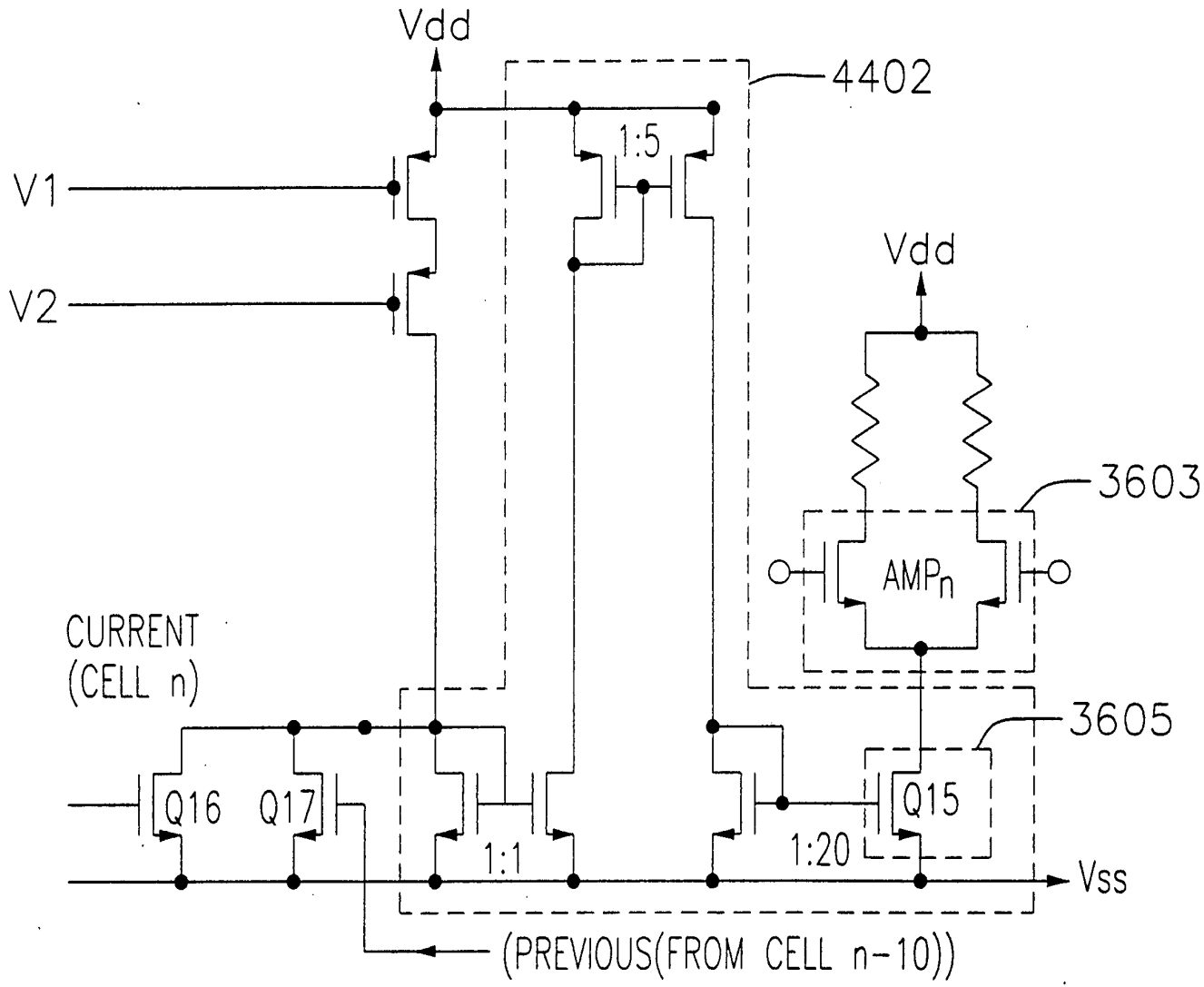

Vdd
4402
1:5
V1
V2
Vdd
3603
AMPn
CURRENT
(CELL n)
3605
Q16
Q17
1:1
Q15
1:20
Vss
(PREVIOUS(FROM CELL n-10))

FIG. 45A

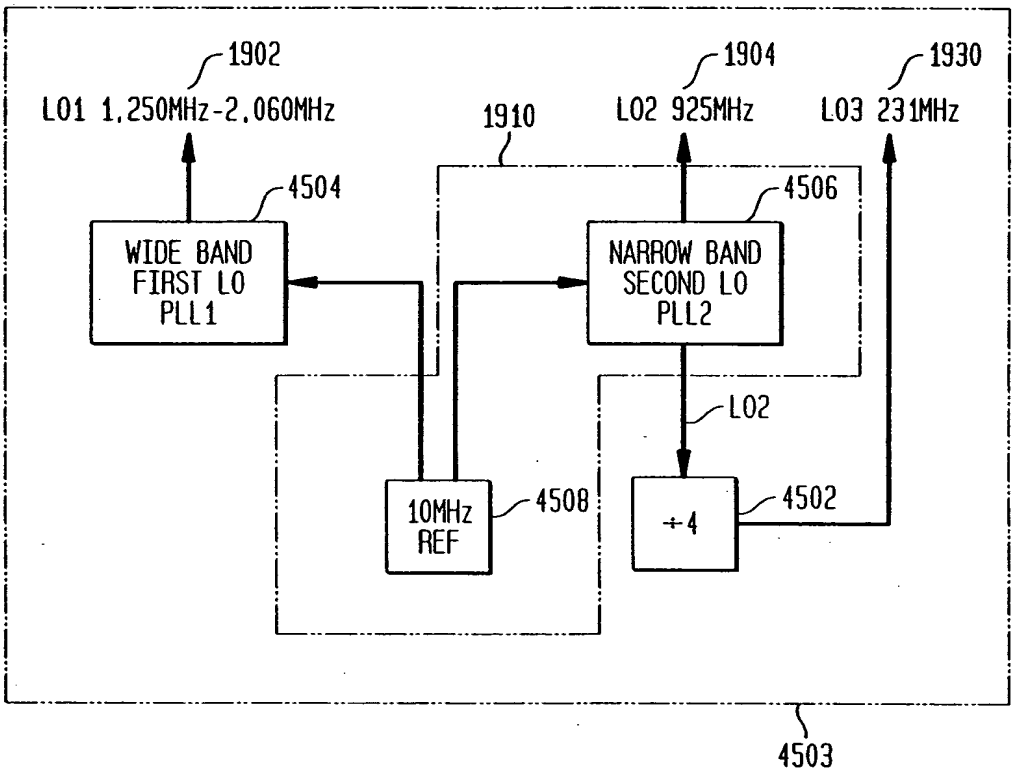

1902
LO1 1,250MHz-2,060MHz
1910
1904
LO2 925MHz
1930
LO3 231MHz
4504
WIDE BAND
FIRST LO
PLL1
4506
NARROW BAND
SECOND LO
PLL2
LO2
10MHz
REF
4508
÷4
4502
4503

FIG. 45B

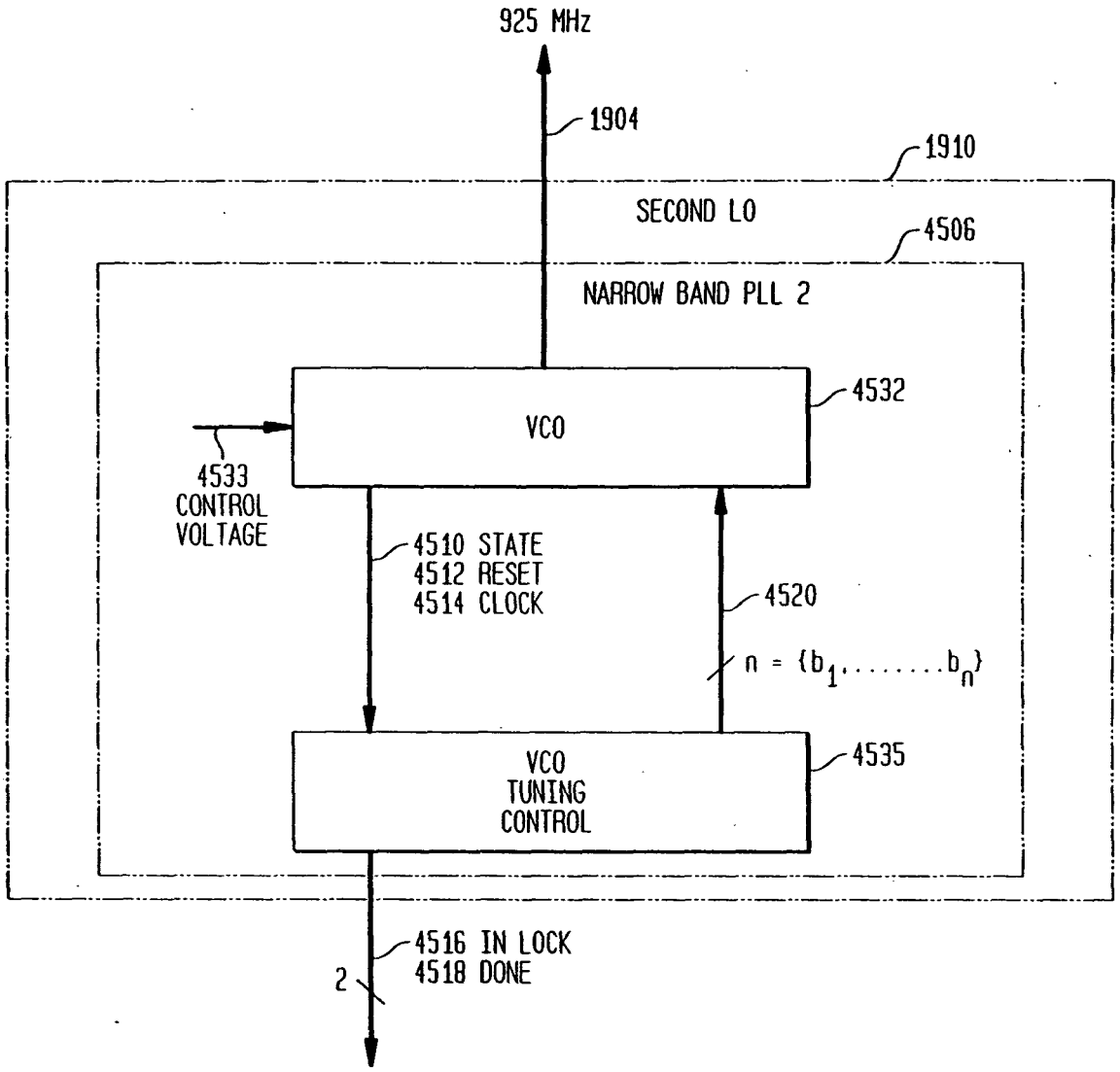

925 MHz
1904
1910
SECOND LO
4506
NARROW BAND PLL 2
4532
VCO
4533
CONTROL
VOLTAGE
4510 STATE
4512 RESET
4514 CLOCK
4520
n = {b1,.....bn}
4535
VCO
TUNING
CONTROL
4516 IN LOCK
4518 DONE
2

FIG. 45C

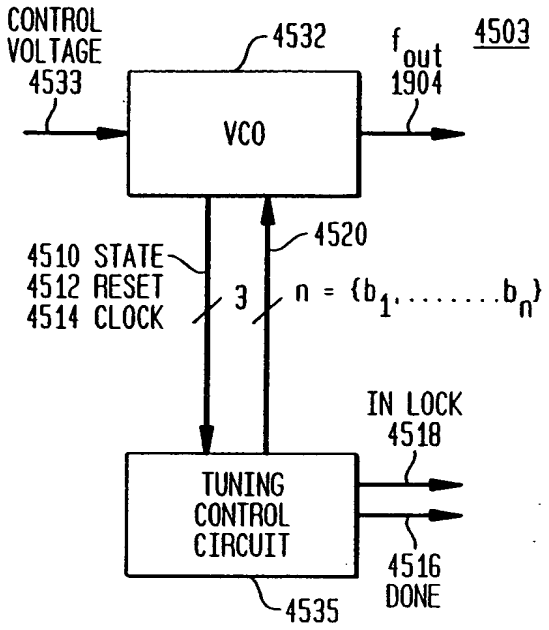


FIG. 45D

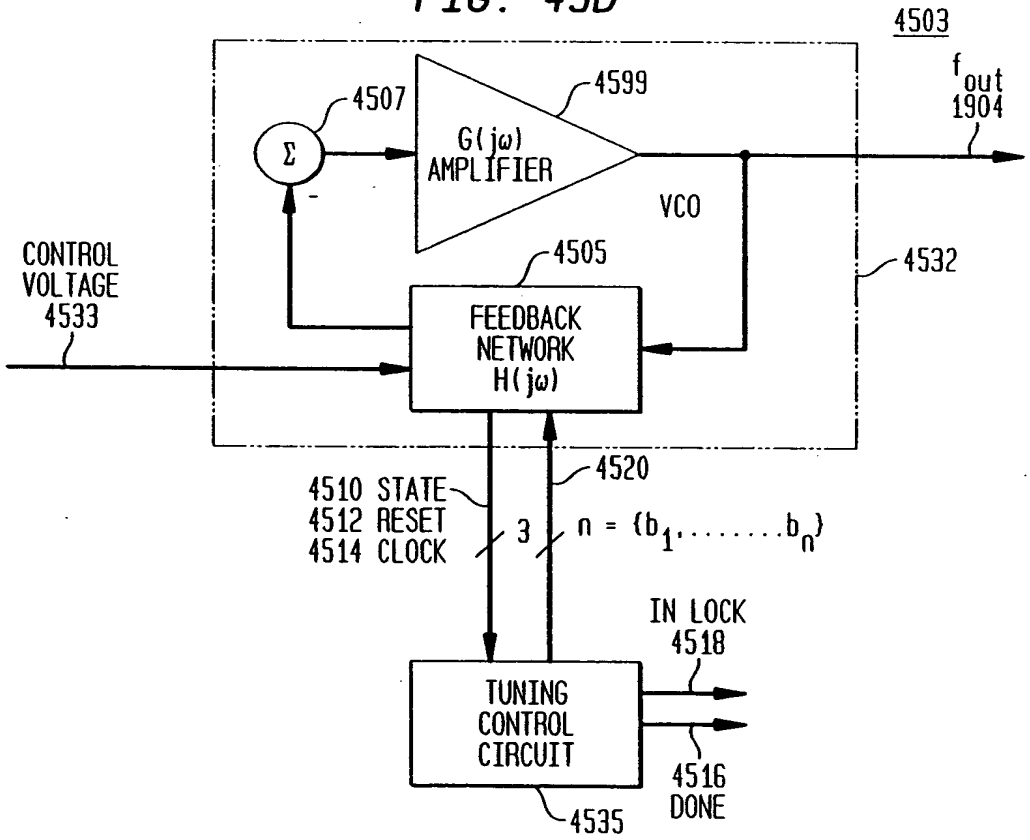


FIG. 45E

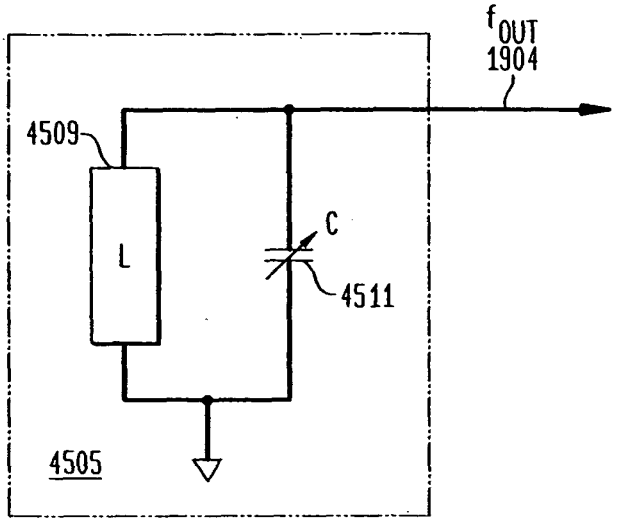


FIG. 45F

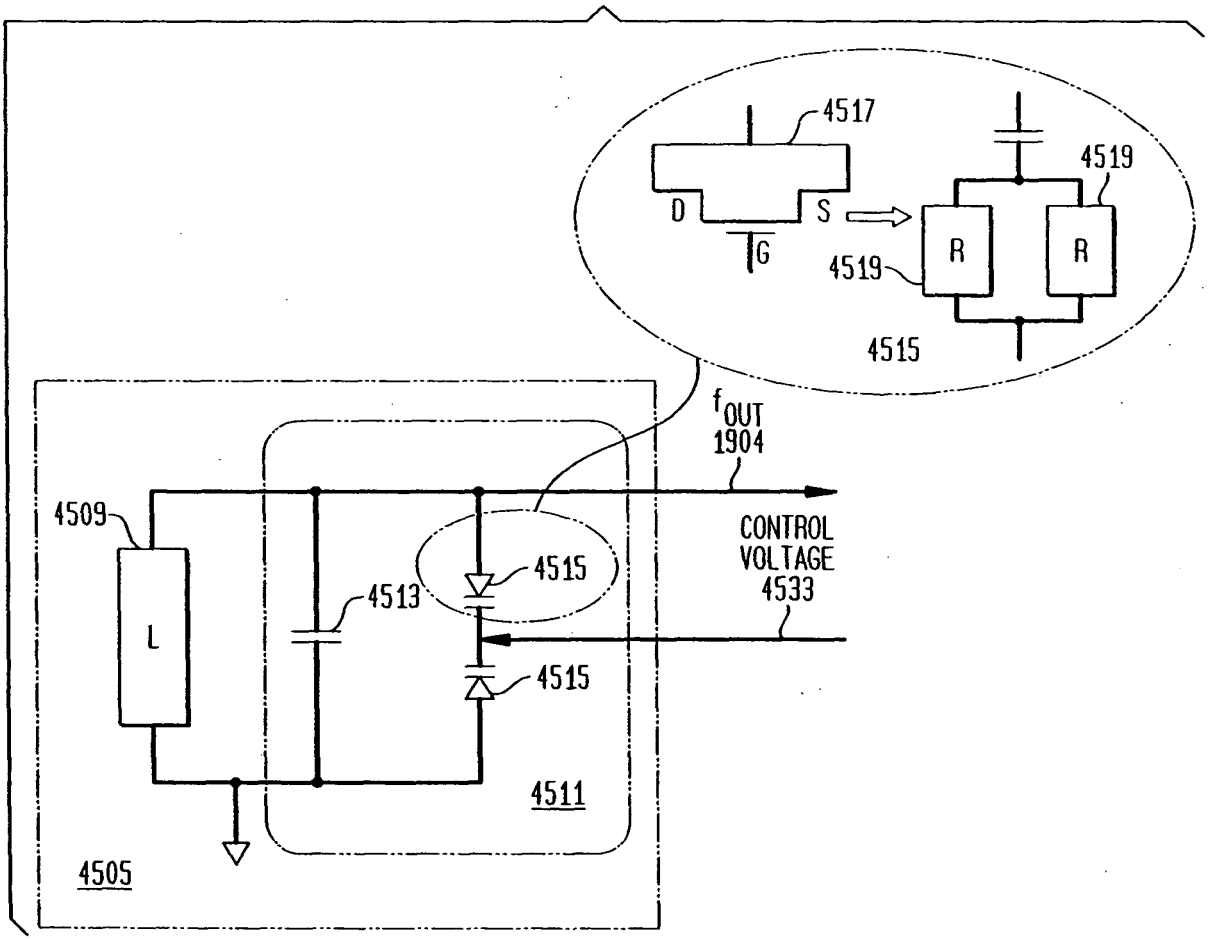


FIG. 45G

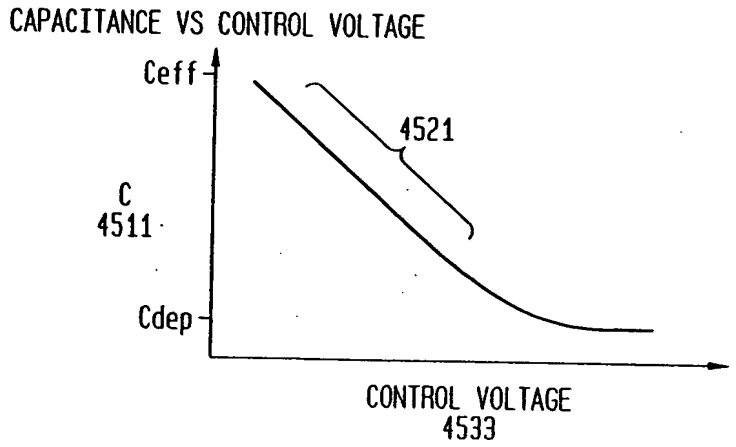


FIG. 45H

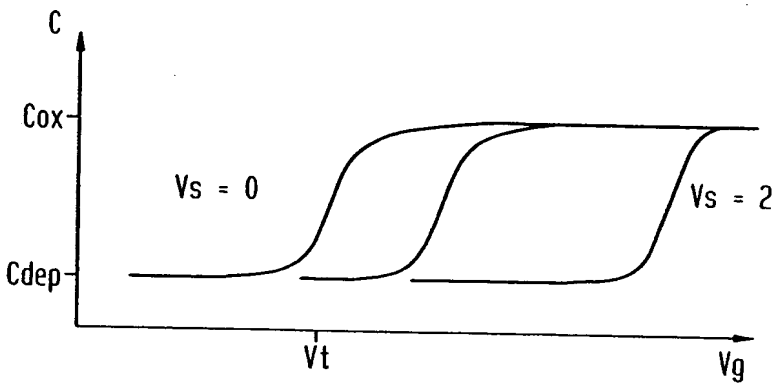


FIG. 45I

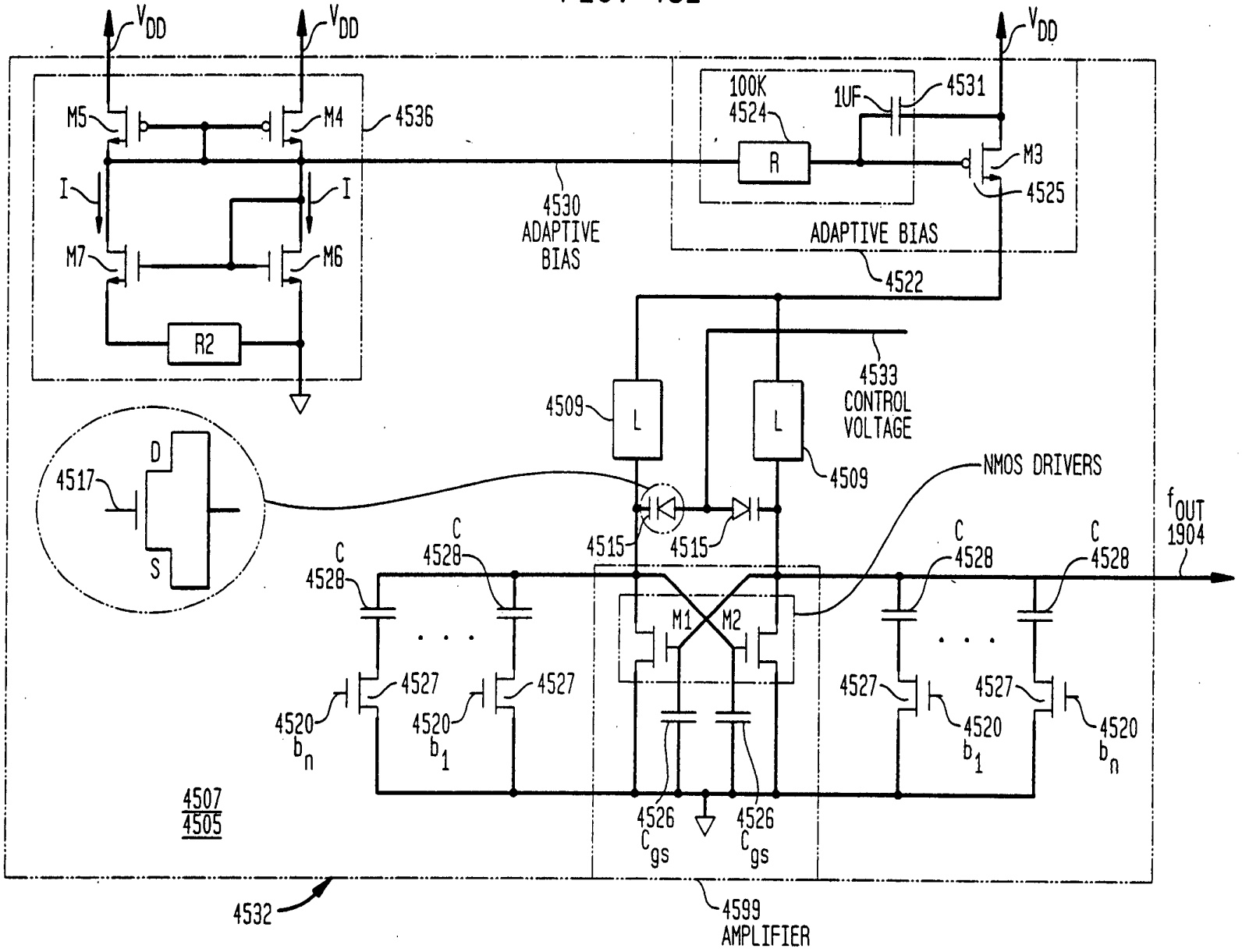

V_{DD}
V_{DD}
V_{DD}
M5
M4
4536
I
I
M7
M6
R2
4530
ADAPTIVE
BIAS
100K
4524
R
1UF
4531
M3
4525
ADAPTIVE BIAS
4522
4533
CONTROL
VOLTAGE
4509
L
L
4509
NMOS DRIVERS
4517
D
S
4515
4515
C
4528
C
4528
C
4528
C
4528
f_{OUT}
1904
M1
M2
4527
4527
4527
4527
4520
b_n
4520
b_1
4520
b_1
4520
b_n
4526
C_{gs}
4526
C_{gs}
4507
4505
4532
4599
AMPLIFIER

FIG. 45J

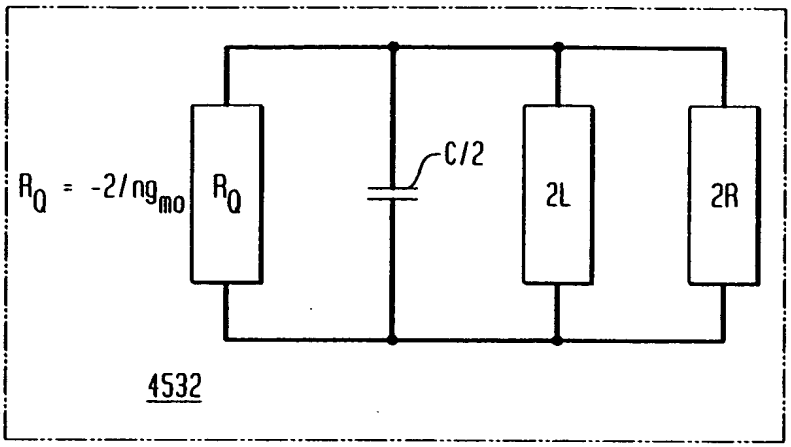


FIG. 45K

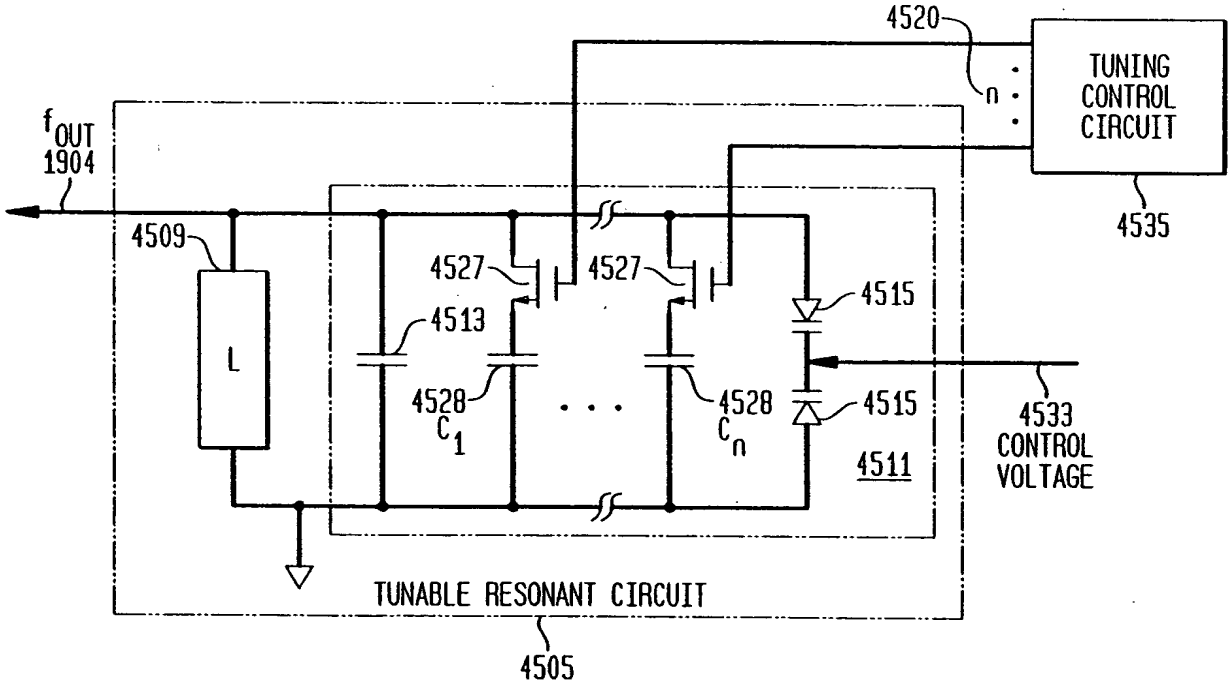


FIG. 46A

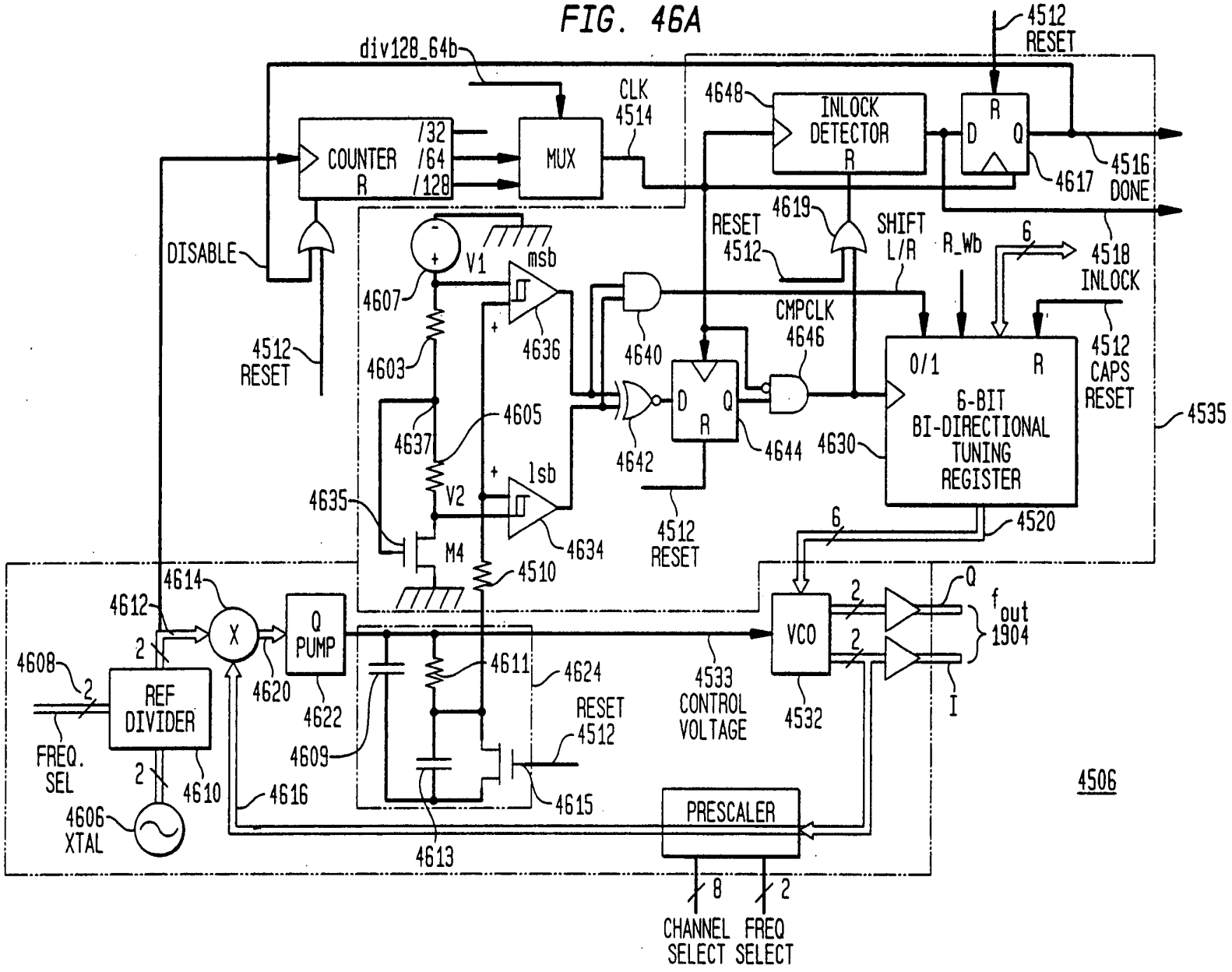

div128_64b
4512 RESET
CLK 4514
4648
INLOCK DETECTOR R
R
D Q
4617
4516 DONE
COUNTER R
/32
/64
/128
MUX
DISABLE
4512 RESET
4619
RESET 4512
SHIFT L/R
R_Wb
6
4518 INLOCK
V1
msb
4607
4636
4640
CMPCLK 4646
4603
4605
4637
D Q
R
4644
4642
0/1
R
6-BIT BI-DIRECTIONAL TUNING REGISTER
4630
4512 CAPS RESET
4535
V2
lsb
4635
M4
4634
4510
4512 RESET
6
4520
4614
4612
X
Q PUMP
2
4608
2
REF DIVIDER
4620
4622
4611
4624
RESET 4512
4609
4533 CONTROL VOLTAGE
VCO
4532
2
2
Q
I
f out 1904
FREQ. SEL
2
4610
4606 XTAL
4616
4615
4613
PRESCALER
4506
8
2
CHANNEL SELECT
FREQ SELECT

FIG. 46B

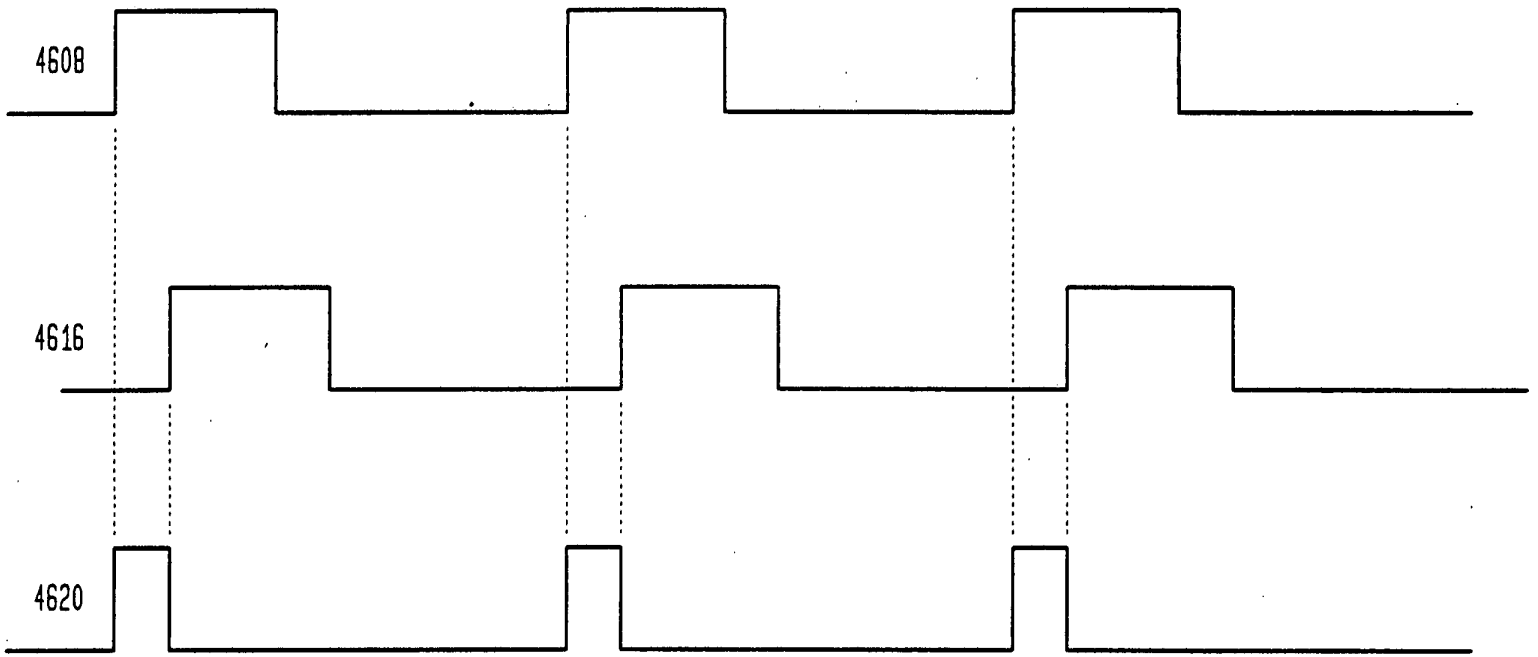


FIG. 47A

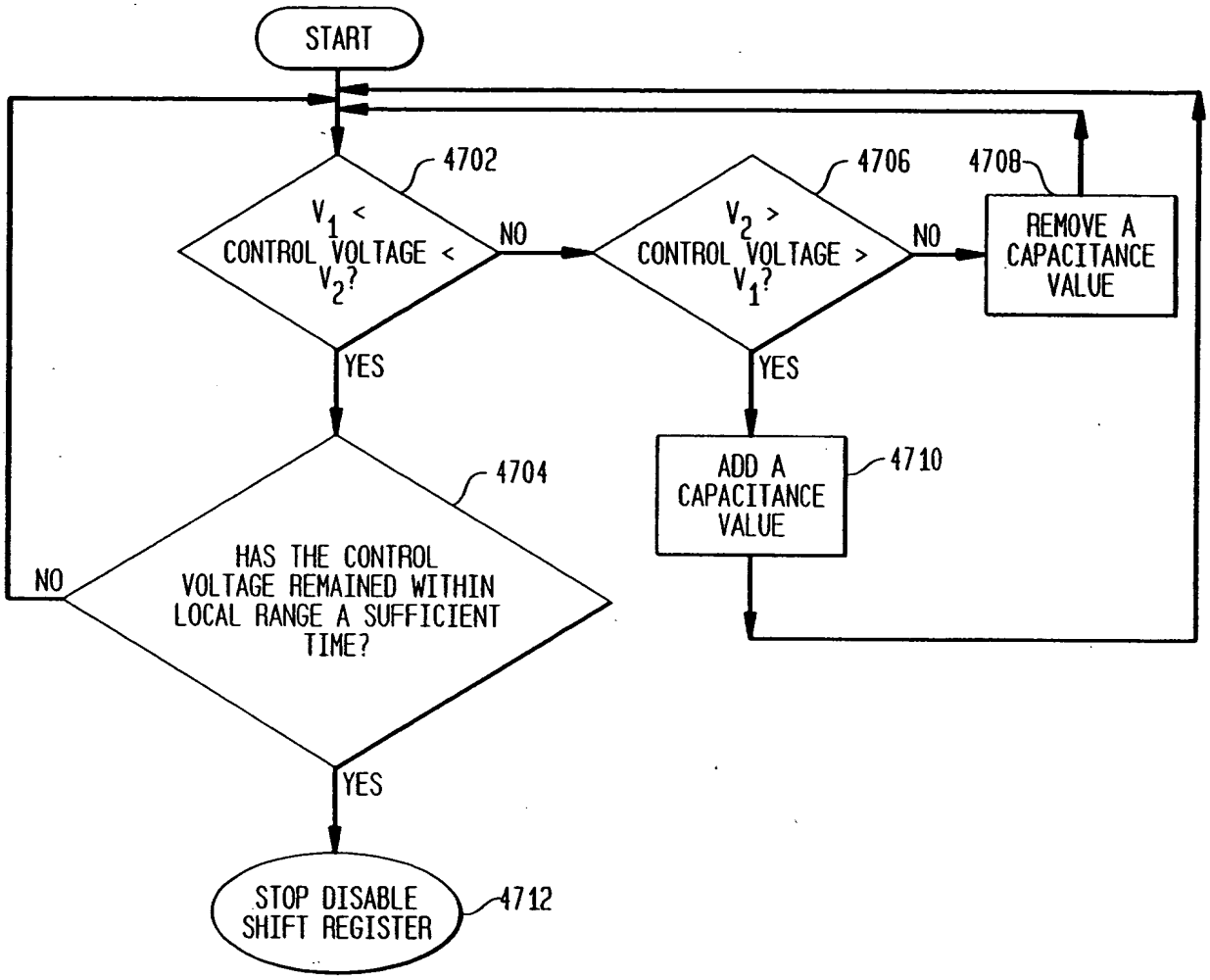

START
4702
V_1 < CONTROL VOLTAGE < V_2?
NO
4706
V_2 > CONTROL VOLTAGE > V_1?
NO
4708
REMOVE A CAPACITANCE VALUE
YES
YES
4704
HAS THE CONTROL VOLTAGE REMAINED WITHIN LOCAL RANGE A SUFFICIENT TIME?
NO
ADD A CAPACITANCE VALUE
4710
YES
STOP DISABLE SHIFT REGISTER
4712

FIG. 47B

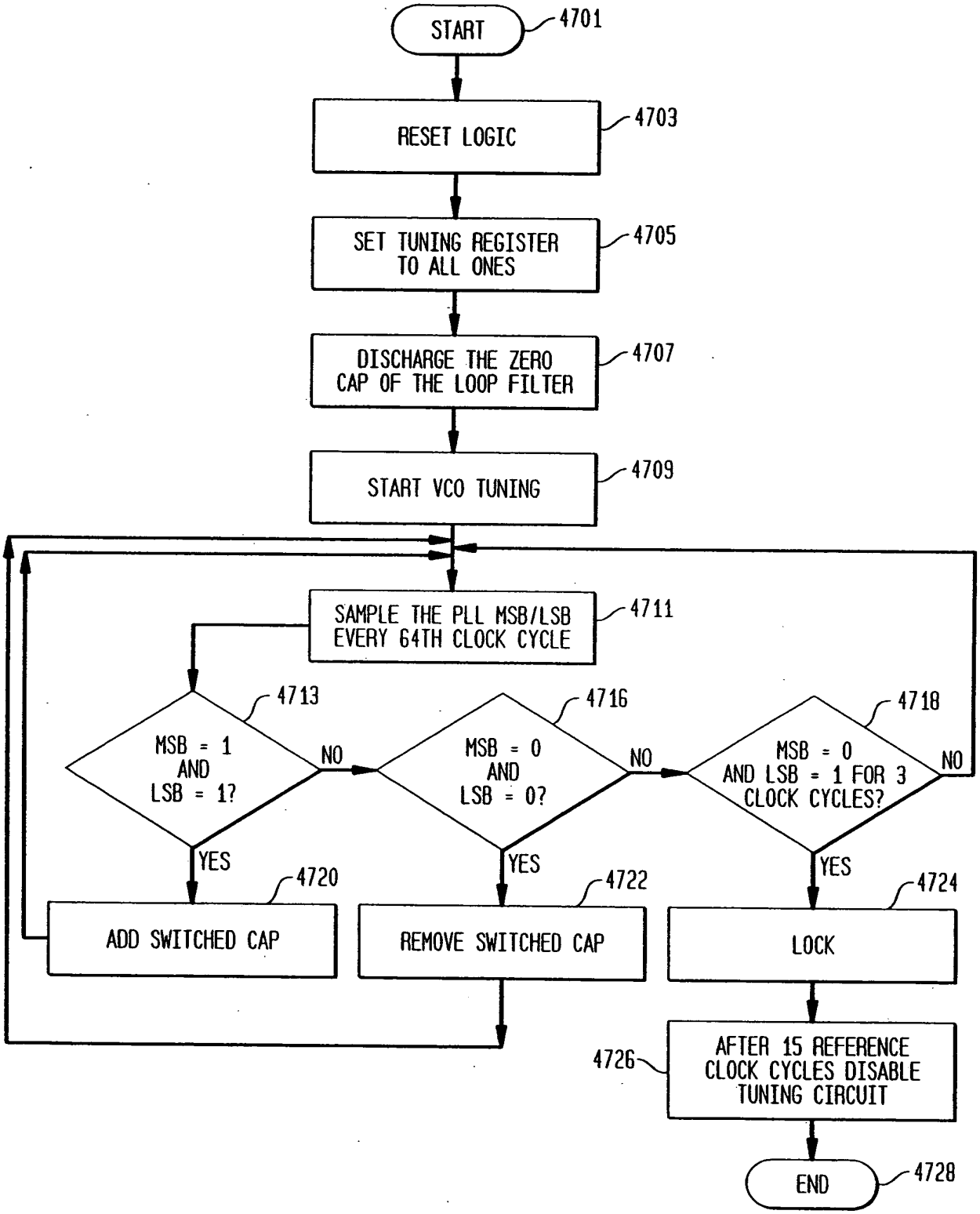

START
4701
RESET LOGIC
4703
SET TUNING REGISTER TO ALL ONES
4705
DISCHARGE THE ZERO CAP OF THE LOOP FILTER
4707
START VCO TUNING
4709
SAMPLE THE PLL MSB/LSB EVERY 64TH CLOCK CYCLE
4711
MSB = 1 AND LSB = 1?
4713
NO
MSB = 0 AND LSB = 0?
4716
NO
MSB = 0 AND LSB = 1 FOR 3 CLOCK CYCLES?
4718
NO
YES
ADD SWITCHED CAP
4720
YES
REMOVE SWITCHED CAP
4722
YES
LOCK
4724
AFTER 15 REFERENCE CLOCK CYCLES DISABLE TUNING CIRCUIT
4726
END
4728

FIG. 47C

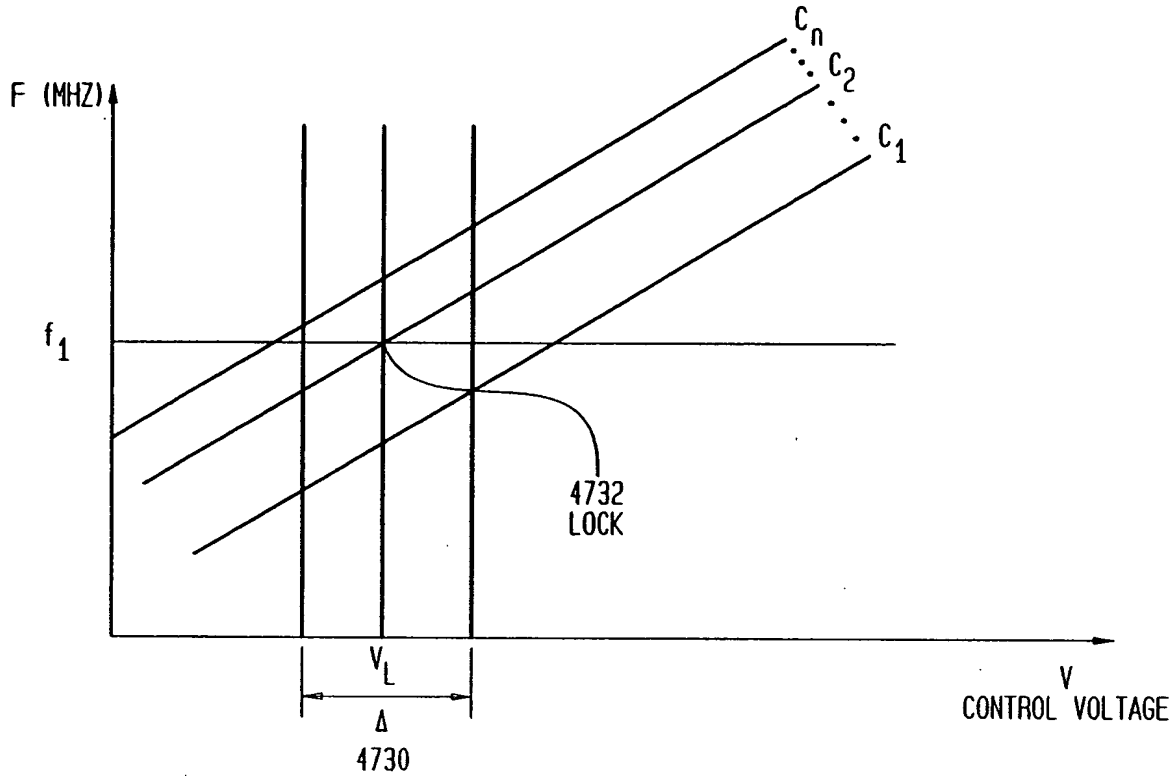


FIG. 47D

REPRESENTATIVE K_{VCO} CURVES

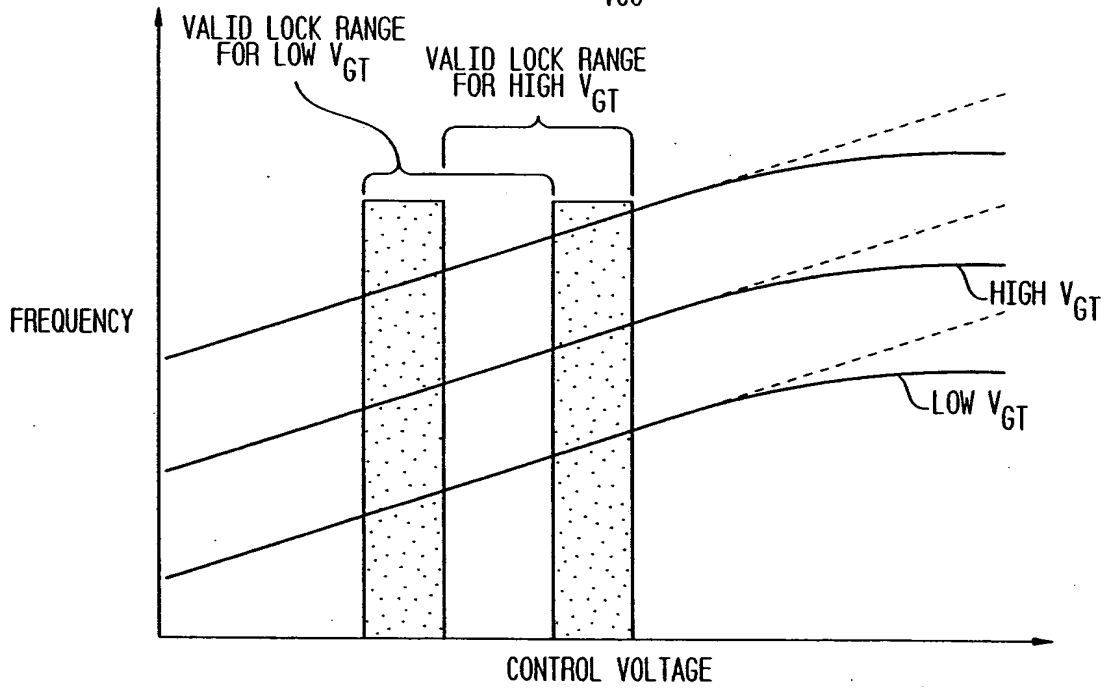


FIG. 48

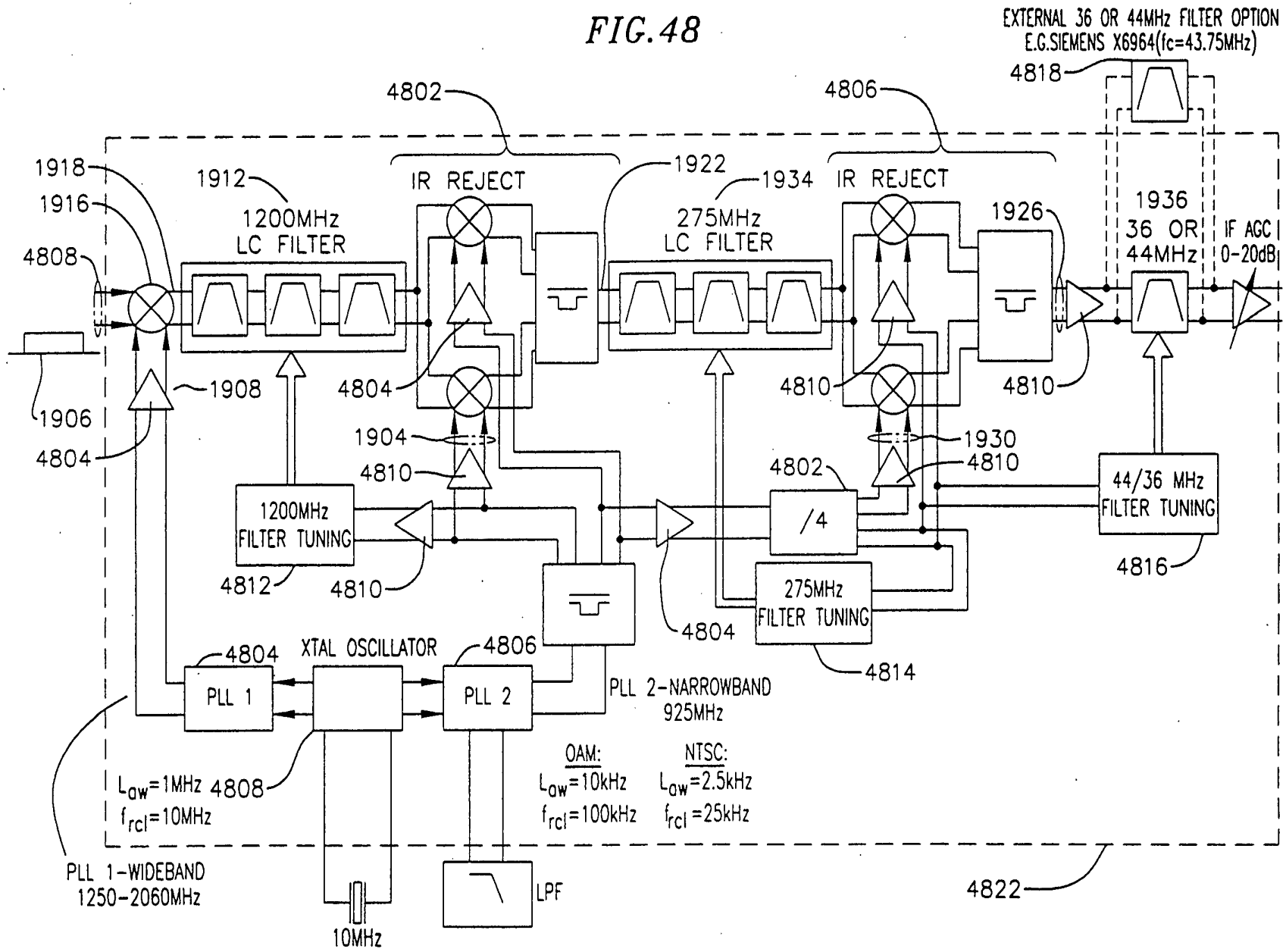

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
4818
4802
4806
1918
1916
1912
1200MHz
LC FILTER
IR REJECT
1922
1934
275MHz
LC FILTER
IR REJECT
1926
1936
36 OR
44MHz
IF AGC
0-20dB
4808
1906
4804
1908
4804
4810
4810
1904
1930
4810
4802
1200MHz
FILTER TUNING
/4
44/36 MHz
FILTER TUNING
4812
4810
4804
275MHz
FILTER TUNING
4816
4814
4804
XTAL OSCILLATOR
4806
PLL 1
PLL 2
PLL 2-NARROWBAND
925MHz
OAM:
L_{aw}=10kHz
f_{rcl}=100kHz
NTSC:
L_{aw}=2.5kHz
f_{rcl}=25kHz
L_{aw}=1MHz 4808
f_{rcl}=10MHz
PLL 1-WIDEBAND
1250-2060MHz
10MHz
LPF
4822

FIG.49

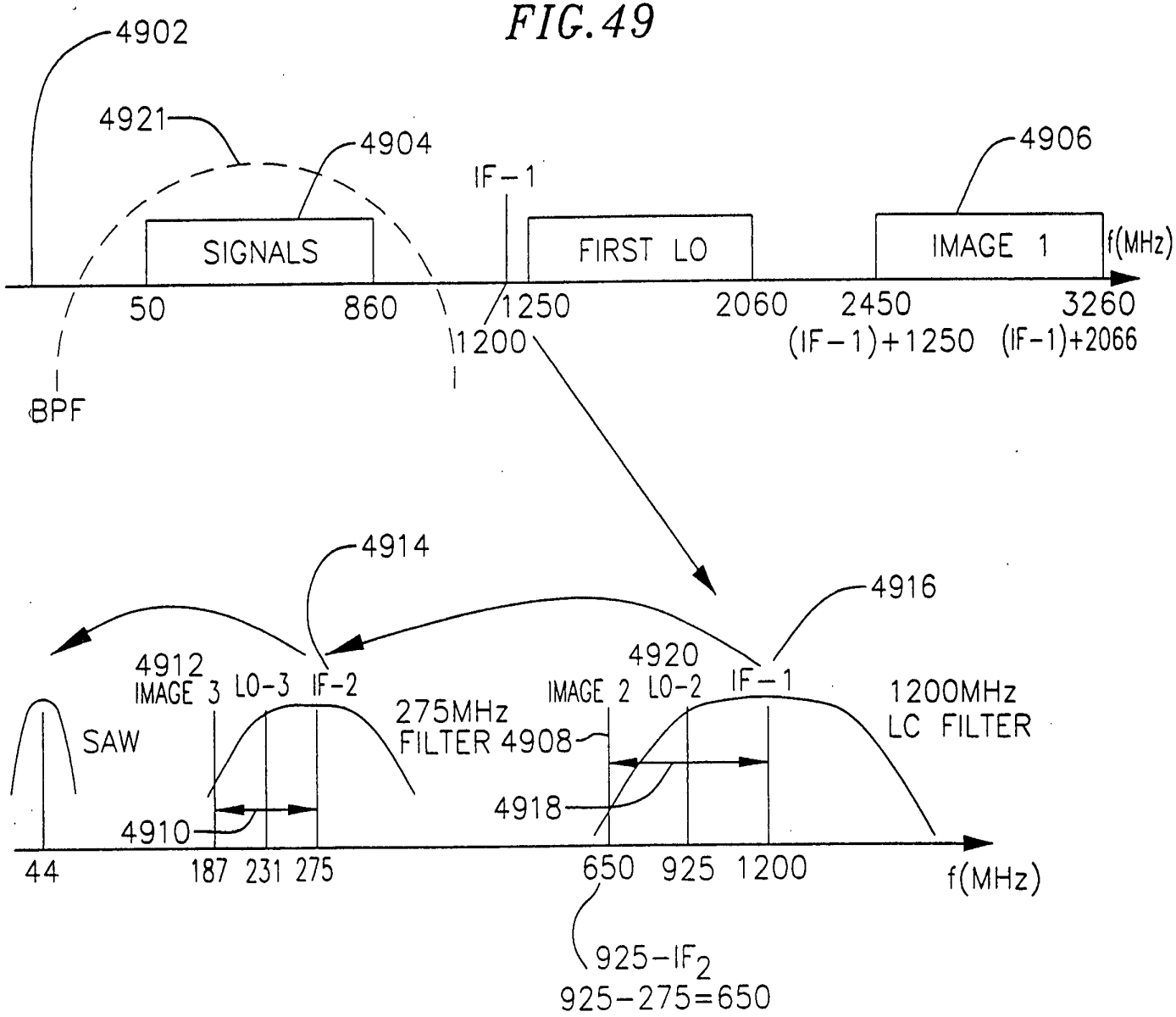

4902
4921
4904
IF-1
4906
SIGNALS
FIRST LO
IMAGE 1
f(MHz)
50
860
1250
2060
2450
3260
1200
(IF-1)+1250
(IF-1)+2066
BPF
4914
4916
4912
IMAGE 3 LO-3 IF-2
4920
IMAGE 2 LO-2 IF-1
1200MHz
LC FILTER
SAW
275MHz
FILTER 4908
4918
4910
44
187 231 275
650 925 1200
f(MHz)
925-IF2
925-275=650

FIG.50

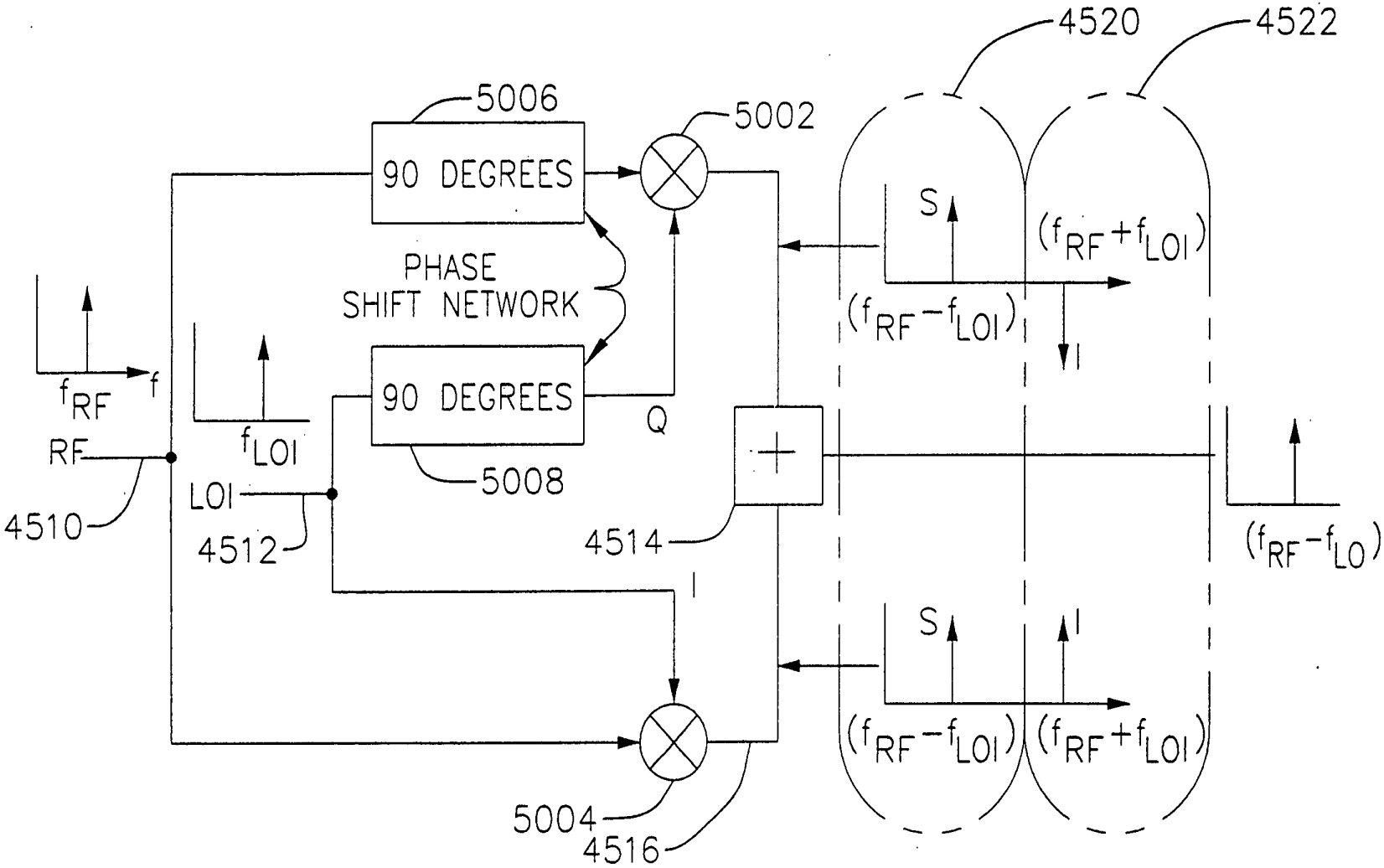

4520
4522
5006
5002
90 DEGREES
PHASE
SHIFT NETWORK
90 DEGREES
5008
Q
I
S
I
S
I
f_{RF}
f
f_{LOI}
RF
LOI
4510
4512
4514
4516
5004
$(f_{RF}+f_{LOI})$
$(f_{RF}-f_{LOI})$
$(f_{RF}-f_{LOI})$
$(f_{RF}+f_{LOI})$
$(f_{RF}-f_{LO})$

FIG.51

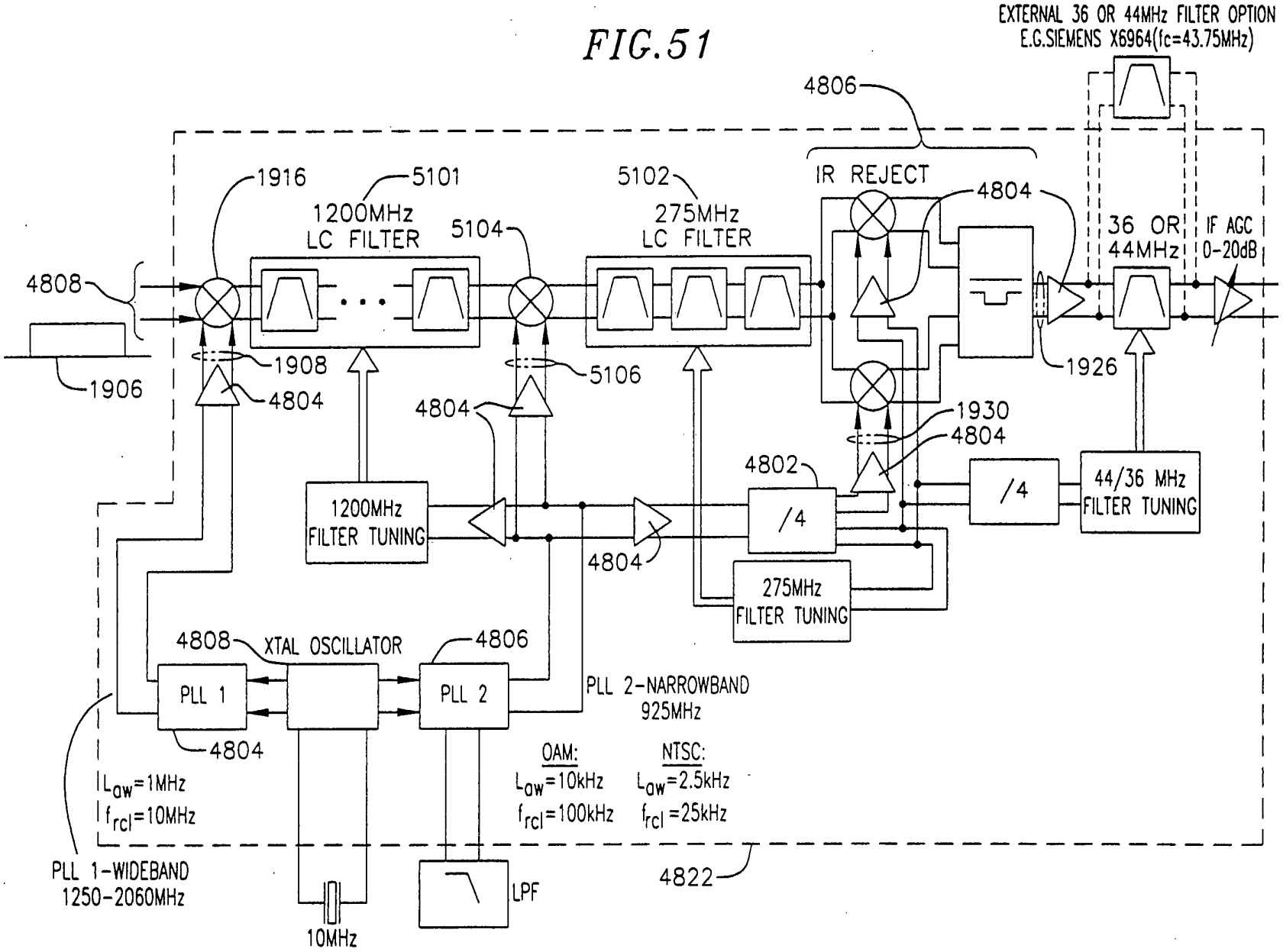

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
4806
IR REJECT
1916
5101
1200MHz
LC FILTER
5104
5102
275MHz
LC FILTER
4804
36 OR
44MHz
IF AGC
0-20dB
4808
1908
5106
1926
1906
4804
4804
1930
4804
4802
/4
/4
44/36 MHz
FILTER TUNING
1200MHz
FILTER TUNING
4804
275MHz
FILTER TUNING
4808
XTAL OSCILLATOR
4806
PLL 1
PLL 2
PLL 2-NARROWBAND
925MHz
4804
OAM:
L_{aw}=10kHz
f_{rcl}=100kHz
NTSC:
L_{aw}=2.5kHz
f_{rcl}=25kHz
L_{aw}=1MHz
f_{rcl}=10MHz
PLL 1-WIDEBAND
1250-2060MHz
10MHz
LPF
4822

FIG.52

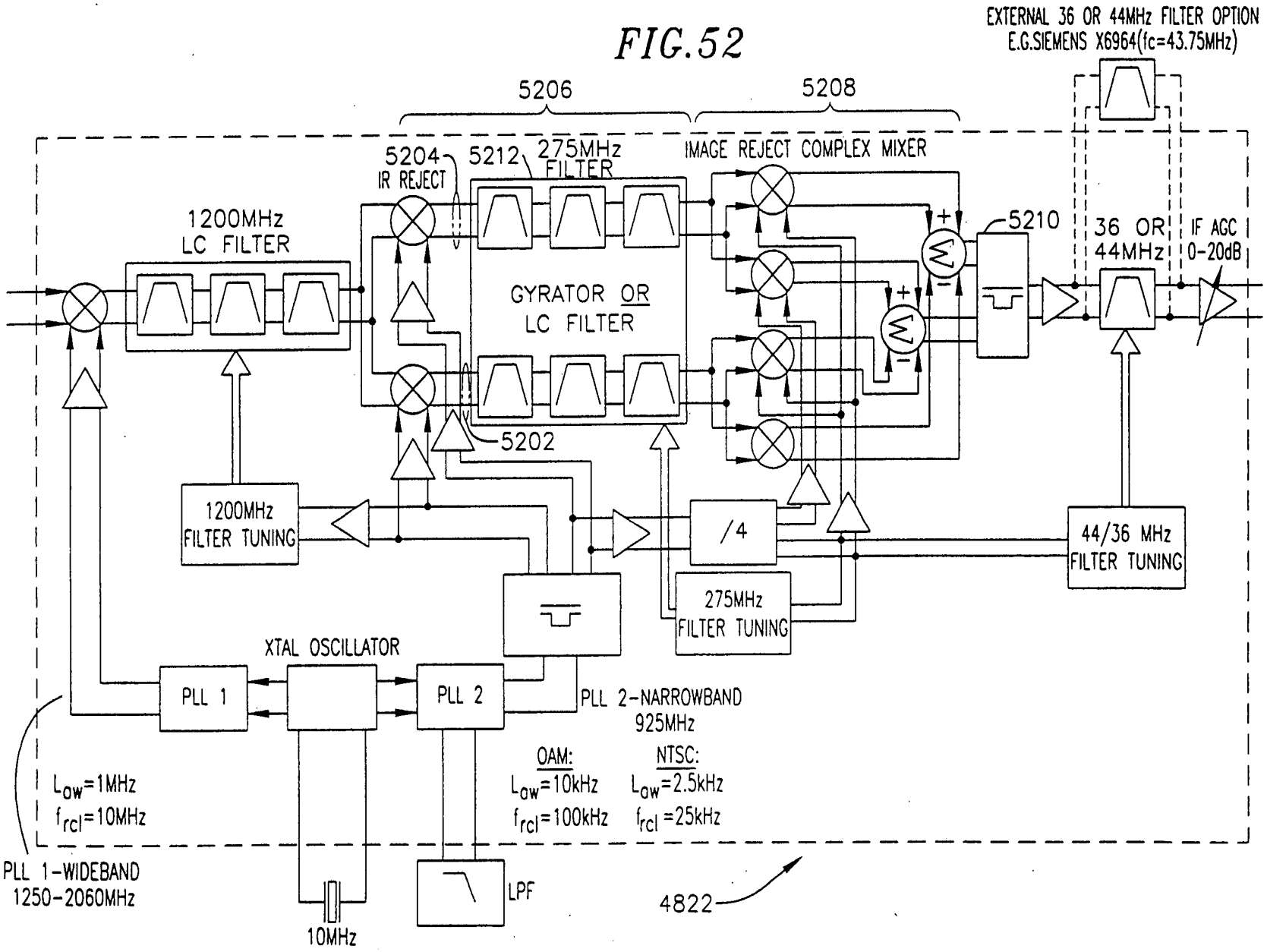

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
5206
5208
5204
IR REJECT
5212
275MHz
FILTER
IMAGE REJECT COMPLEX MIXER
1200MHz
LC FILTER
GYRATOR OR
LC FILTER
5210
36 OR
44MHz
IF AGC
0-20dB
5202
1200MHz
FILTER TUNING
/4
44/36 MHz
FILTER TUNING
275MHz
FILTER TUNING
XTAL OSCILLATOR
PLL 1
PLL 2
PLL 2-NARROWBAND
925MHz
OAM:
L_{ow}=10kHz
f_{rcl}=100kHz
NTSC:
L_{ow}=2.5kHz
f_{rcl}=25kHz
L_{ow}=1MHz
f_{rcl}=10MHz
PLL 1-WIDEBAND
1250-2060MHz
10MHz
LPF
4822

FIG.53

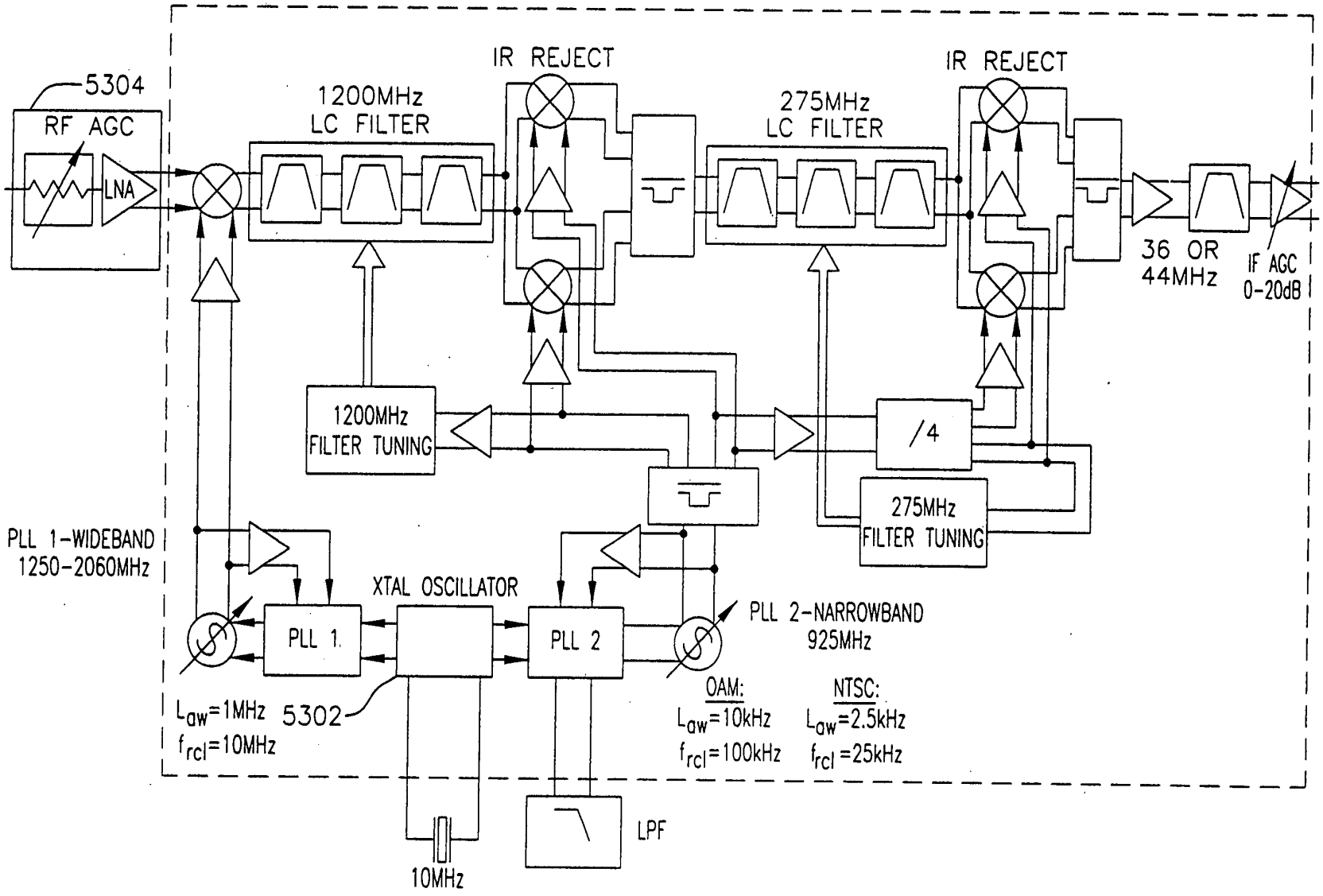

CATV TUNER
5304
RF AGC
LNA
1200MHz
LC FILTER
IR REJECT
275MHz
LC FILTER
IR REJECT
36 OR
44MHz
IF AGC
0-20dB
1200MHz
FILTER TUNING
/4
275MHz
FILTER TUNING
PLL 1-WIDEBAND
1250-2060MHz
XTAL OSCILLATOR
PLL 1
PLL 2
PLL 2-NARROWBAND
925MHz
OAM:
L_{aw}=10kHz
f_{rcl}=100kHz
NTSC:
L_{aw}=2.5kHz
f_{rcl}=25kHz
L_{aw}=1MHz
f_{rcl}=10MHz
5302
10MHz
LPF

FIG.54

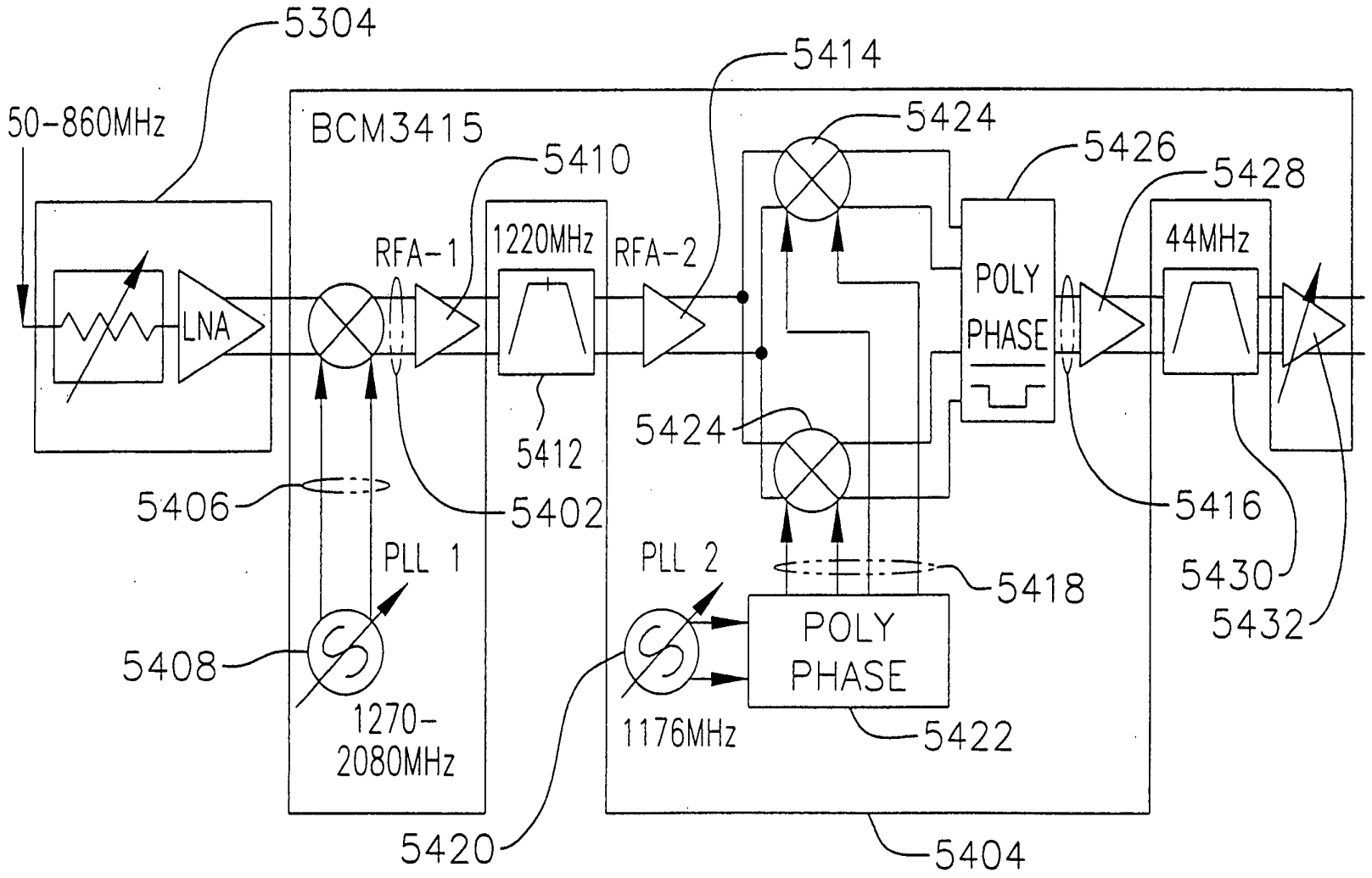

5304
50-860MHz
BCM3415
5414
5424
5426
5428
5410
RFA-1
1220MHz
RFA-2
POLY
PHASE
44MHz
LNA
5412
5424
5406
5402
5416
PLL 1
PLL 2
5418
5430
5432
5408
POLY
PHASE
1270-
2080MHz
1176MHz
5422
5420
5404

FIG.55

SET-TOP BOX

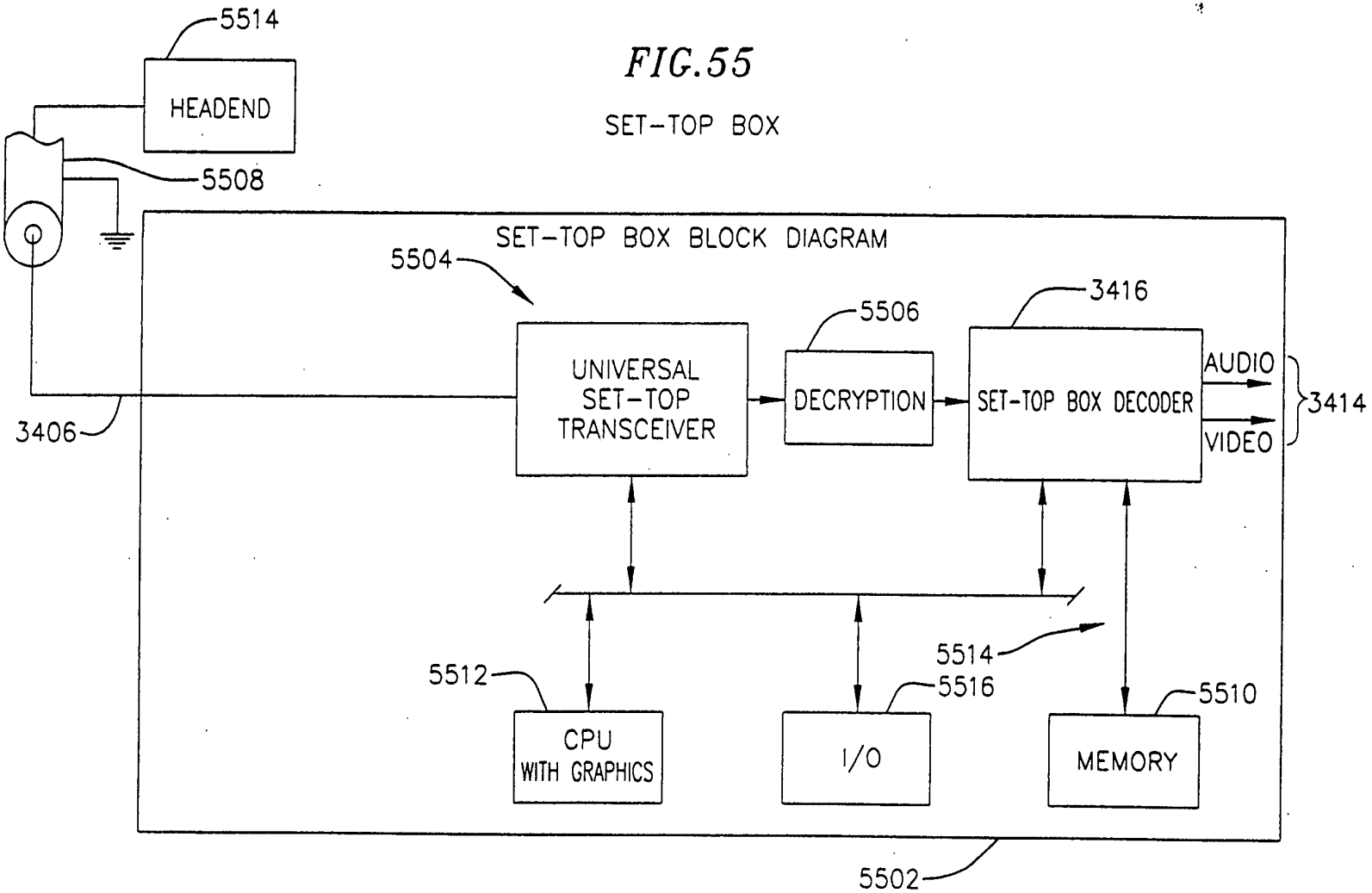


FIG.56

TELEVISION

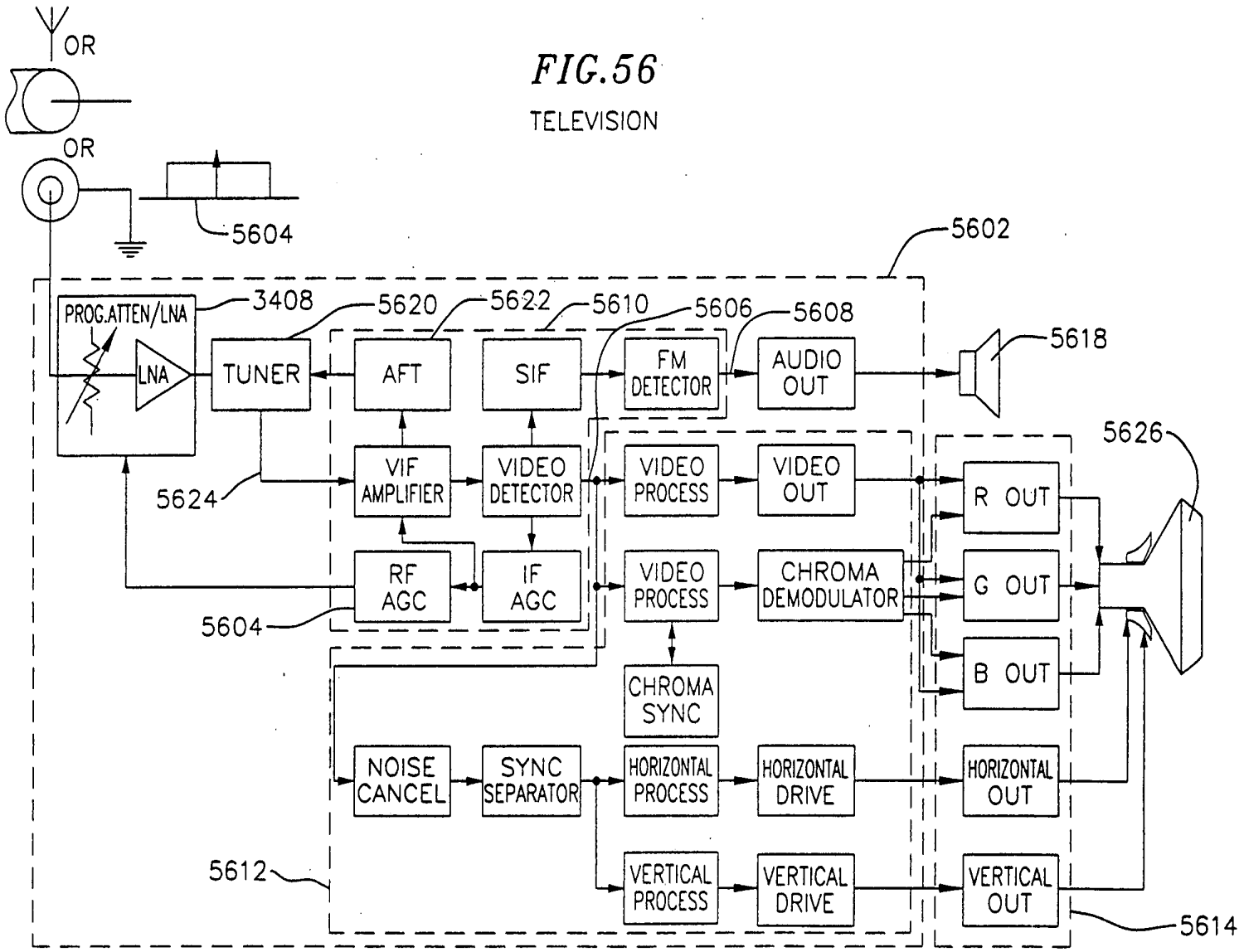


FIG.57

VCR BLOCK DIAGRAM

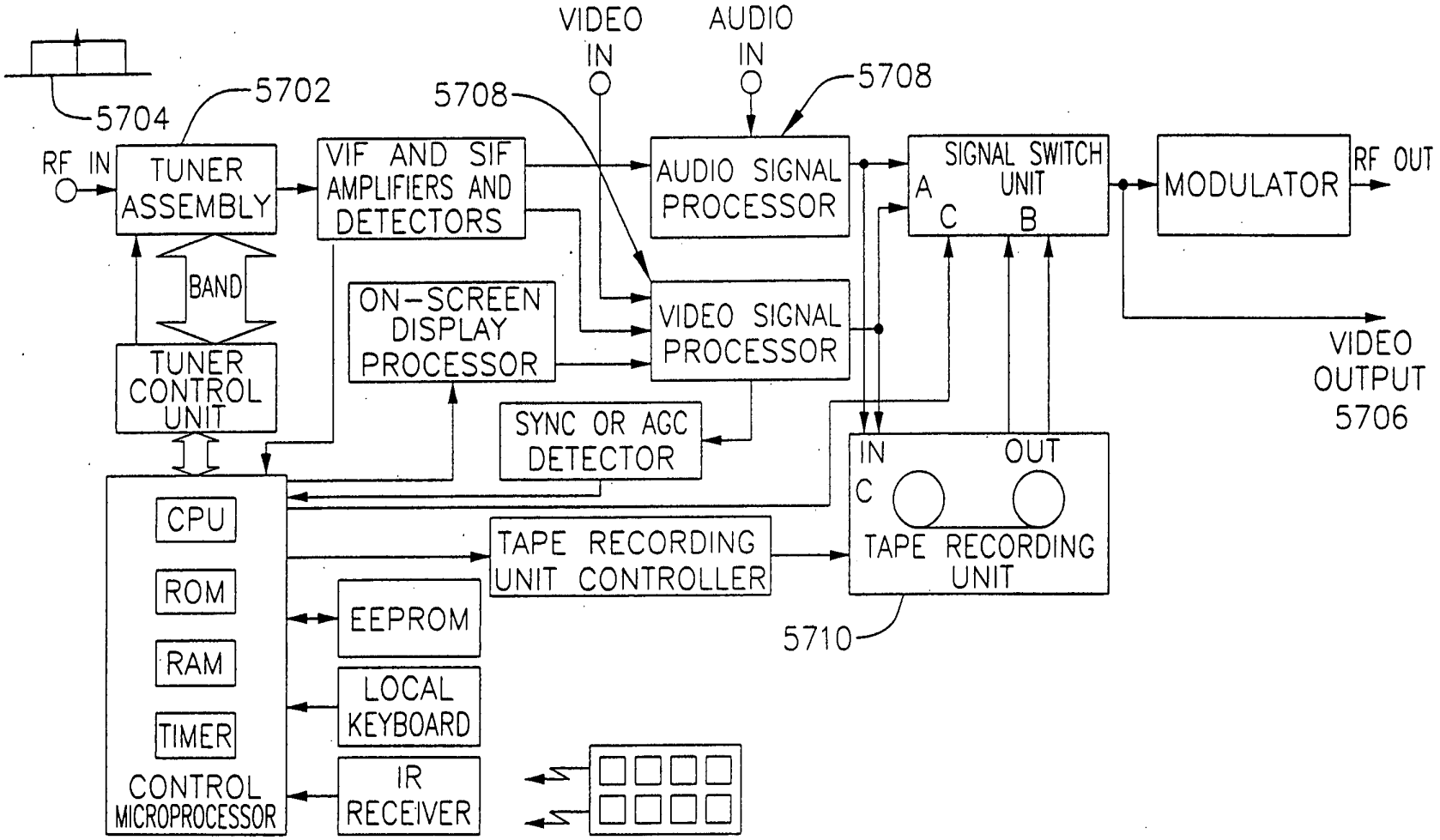


FIG.58

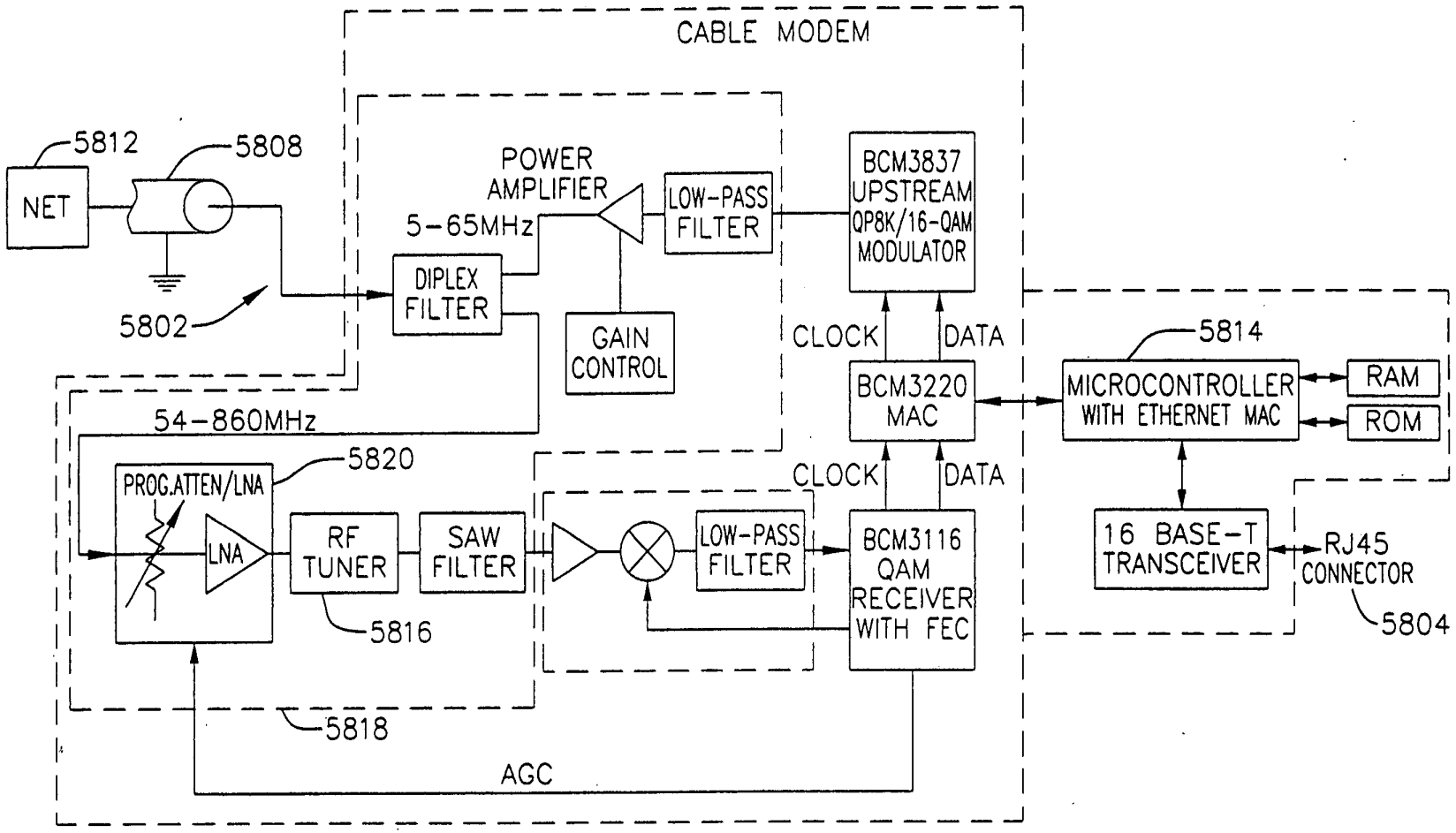

CABLE MODEM
5812
5808
NET
5802
POWER AMPLIFIER
5-65MHz
DIPLEX FILTER
GAIN CONTROL
LOW-PASS FILTER
BCM3837 UPSTREAM QP8K/16-QAM MODULATOR
CLOCK
DATA
BCM3220 MAC
5814
MICROCONTROLLER WITH ETHERNET MAC
RAM
ROM
54-860MHz
5820
PROG.ATTEN/LNA
LNA
RF TUNER
SAW FILTER
LOW-PASS FILTER
BCM3116 QAM RECEIVER WITH FEC
16 BASE-T TRANSCEIVER
RJ45 CONNECTOR
5804
5816
5818
AGC

FIG.59

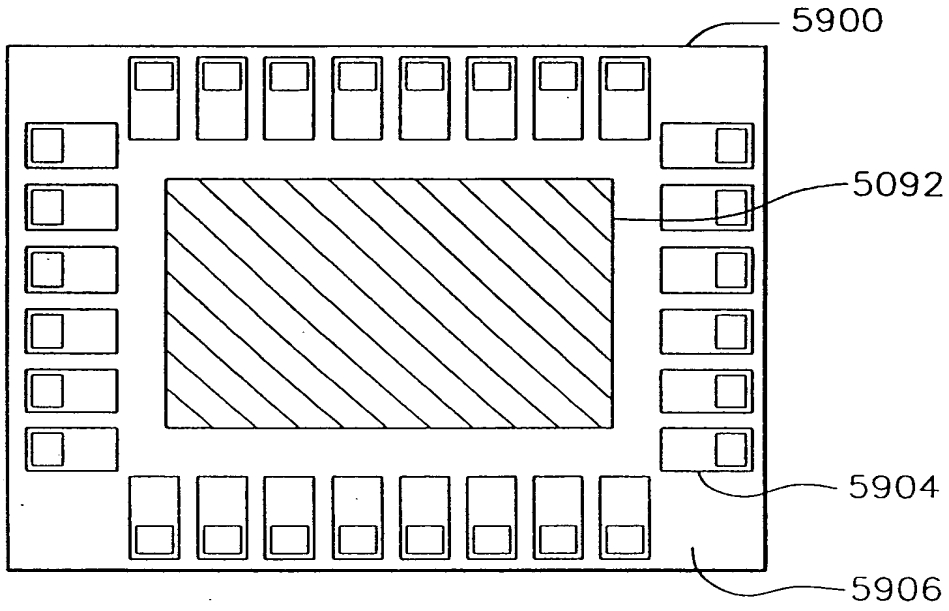


FIG.60

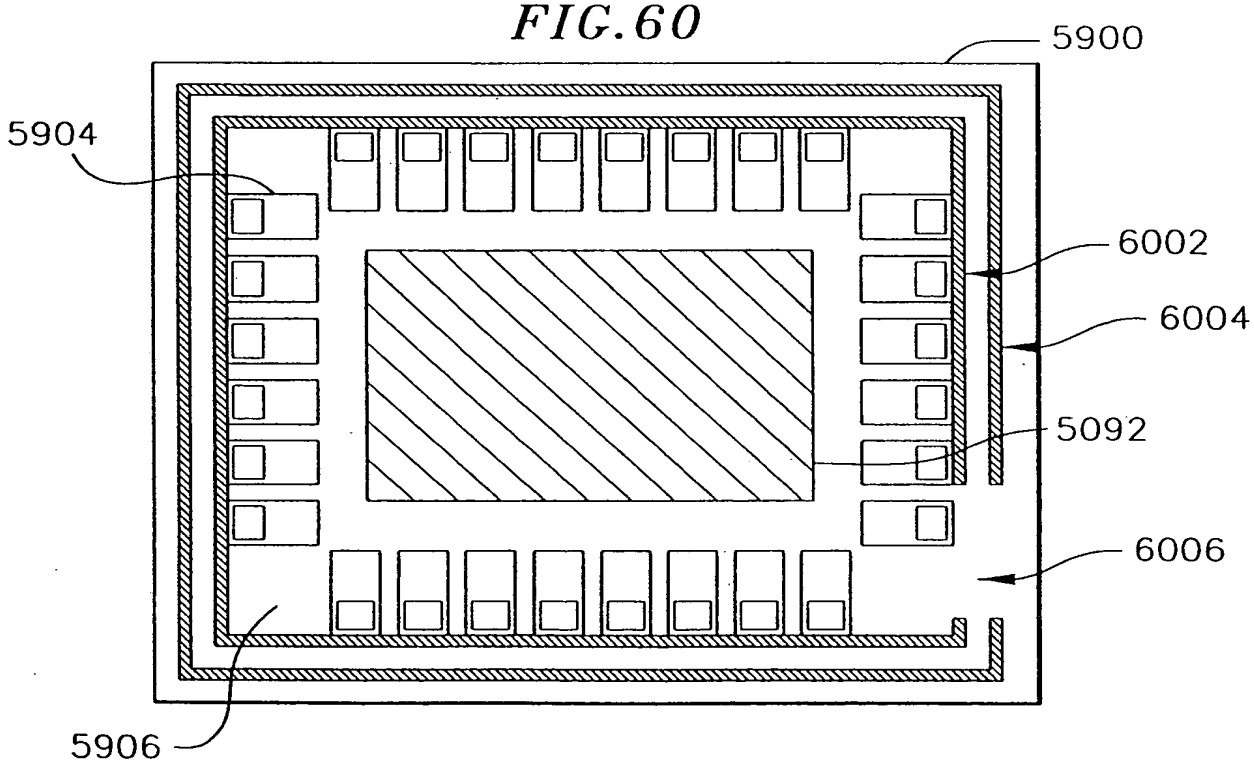


FIG. 61

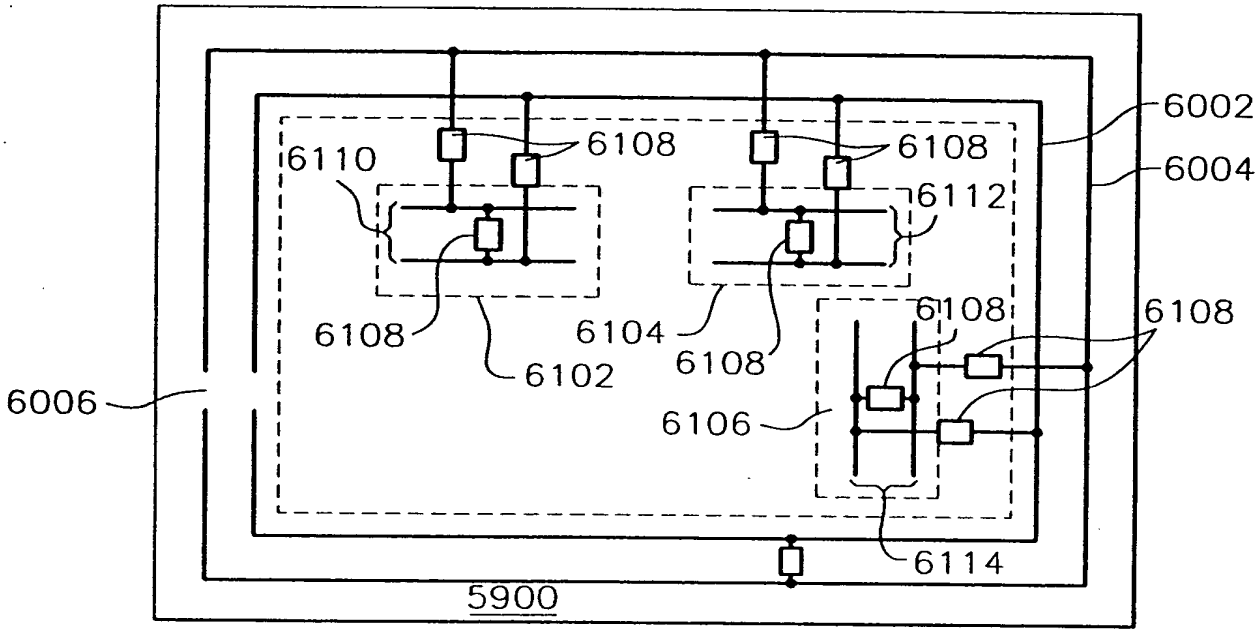

6002
6004
6110
6108
6108
6112
6108
6104
6108
6108
6102
6006
6106
6114
5900

FIG. 62

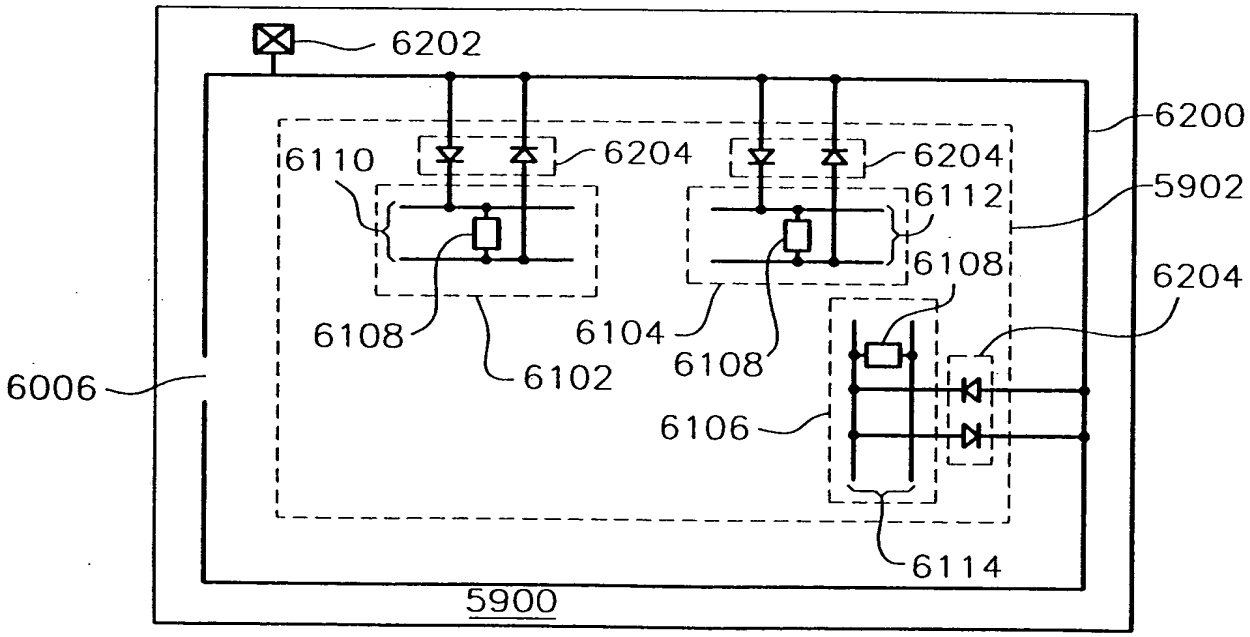

6202
6200
6110
6204
6204
6112
5902
6108
6204
6108
6104
6108
6102
6006
6106
6114
5900

FIG. 63

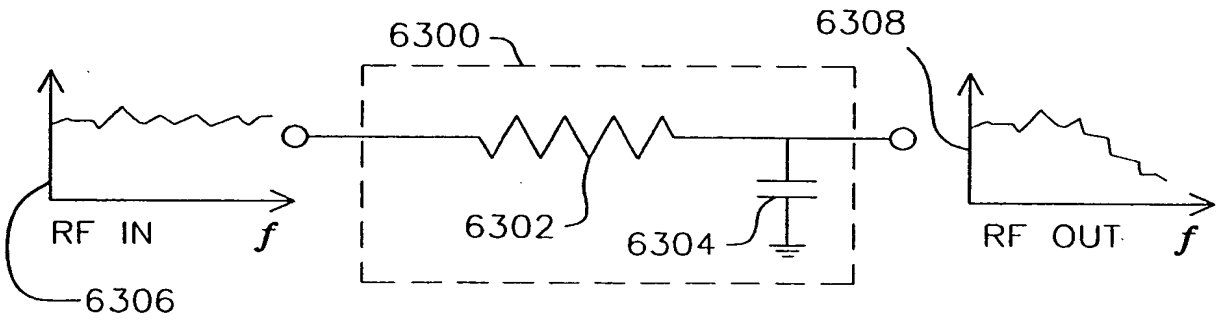


FIG. 64

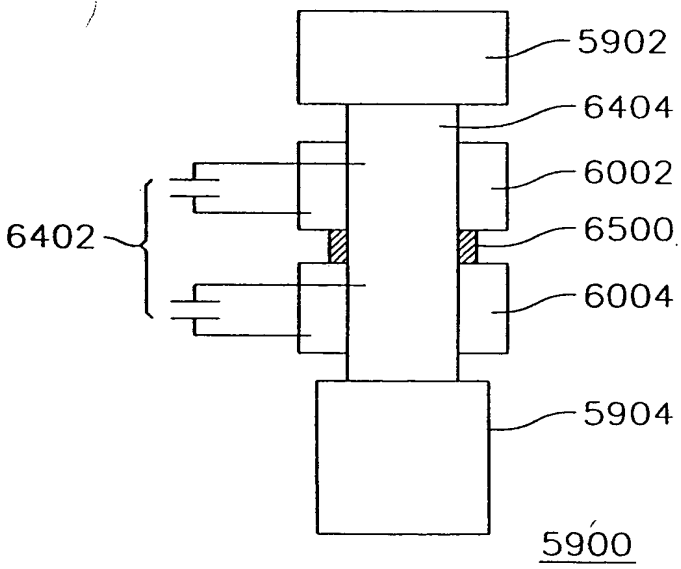


FIG. 65

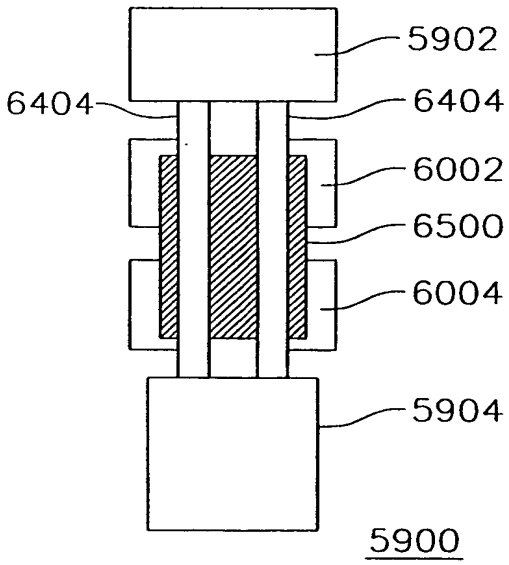


FIG. 66

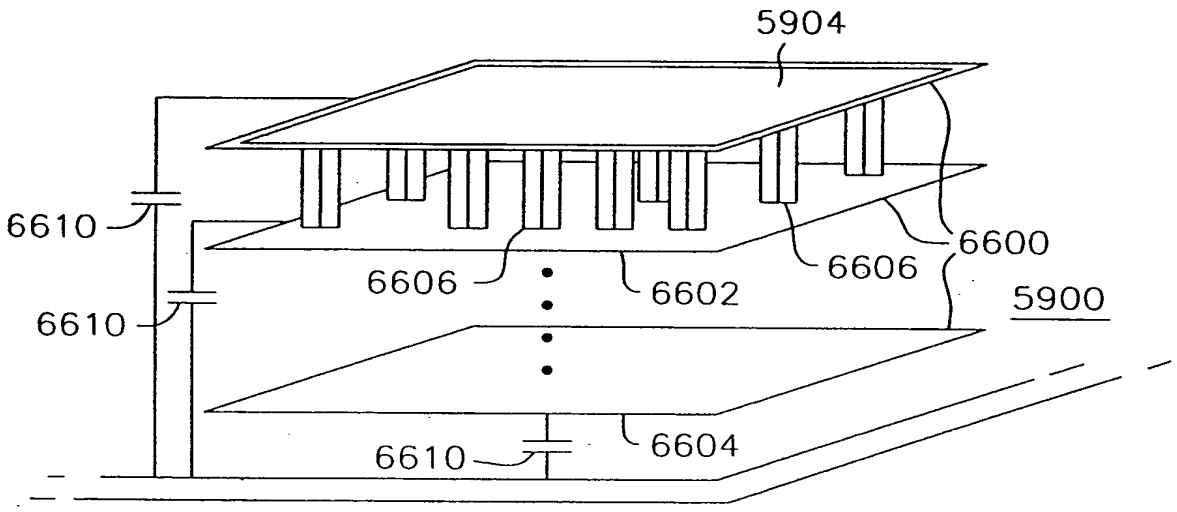

5904
6610
6610
6606
6602
6606
6600
5900
6610
6604

FIG. 67

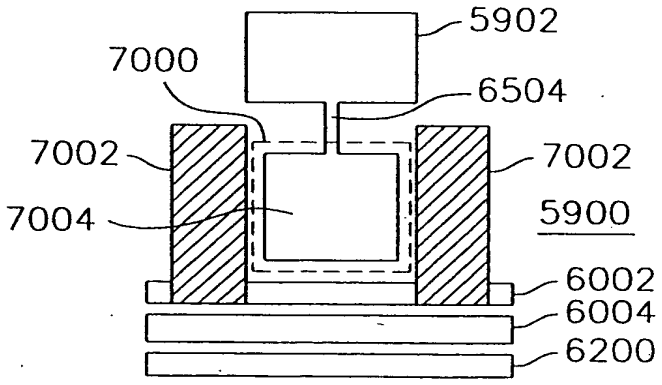

5902
7000
6504
7002
7002
7004
5900
6002
6004
6200

FIG.68

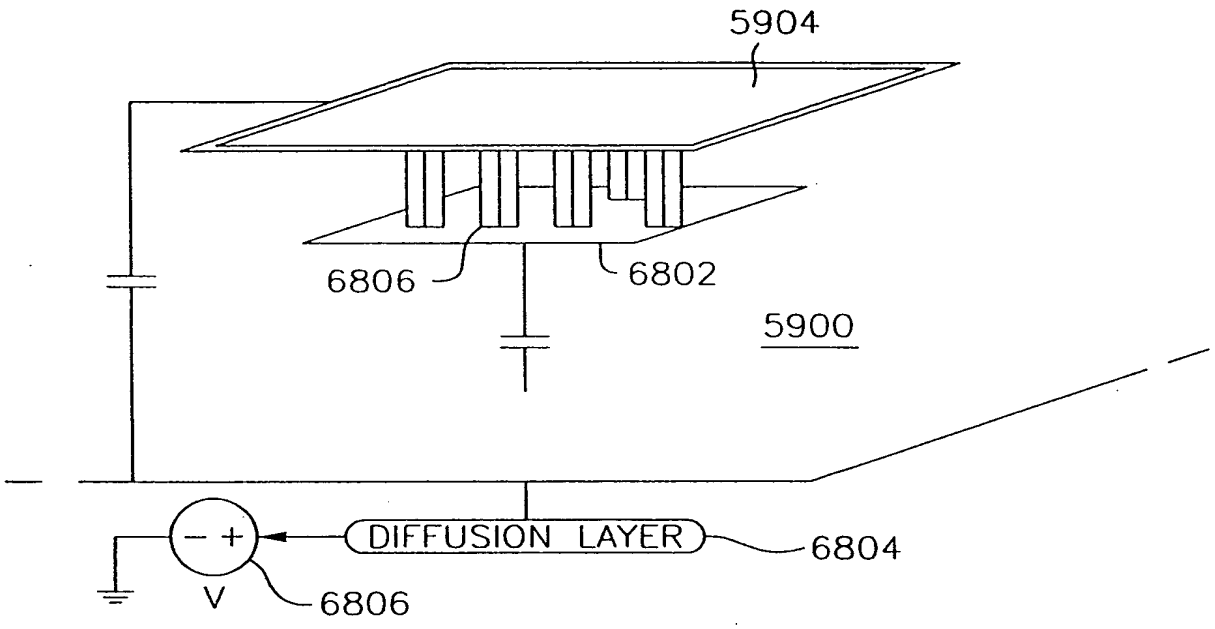


FIG.69a
PRIOR ART

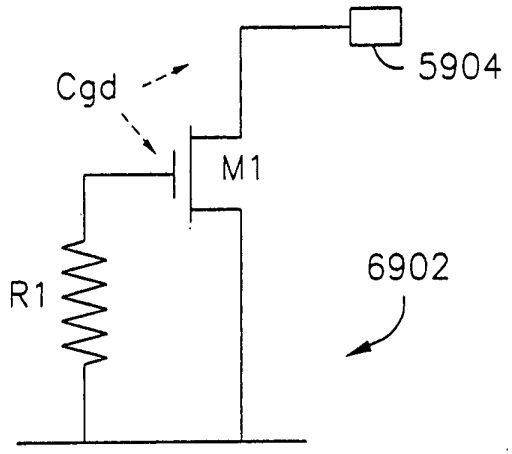


FIG.69b
PRIOR ART

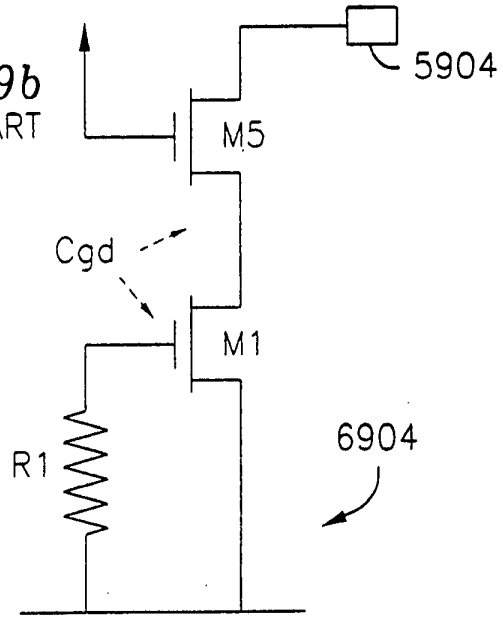


FIG.69c
PRIOR ART

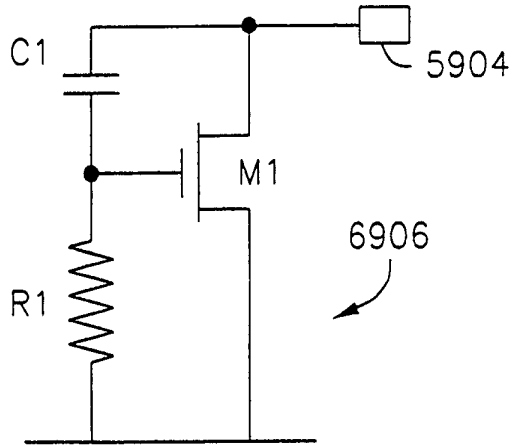


FIG.69d
PRIOR ART

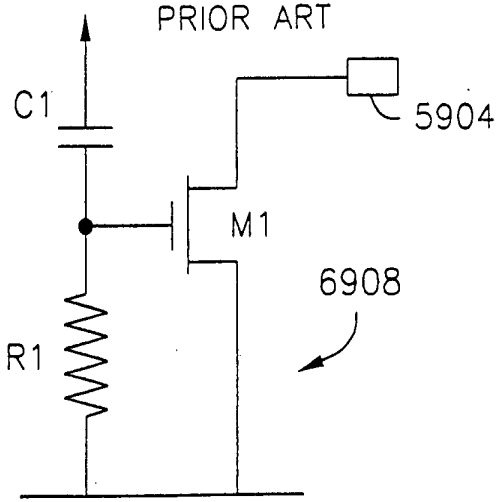


FIG.69e
PRIOR ART

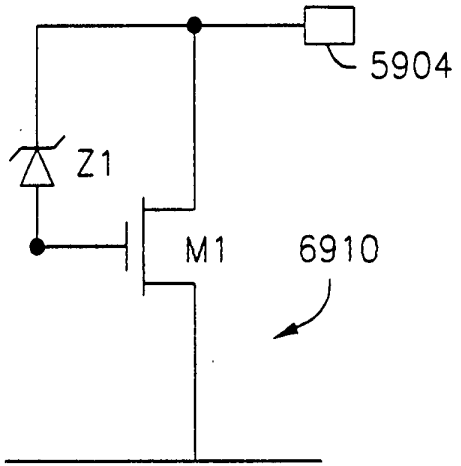


FIG. 70

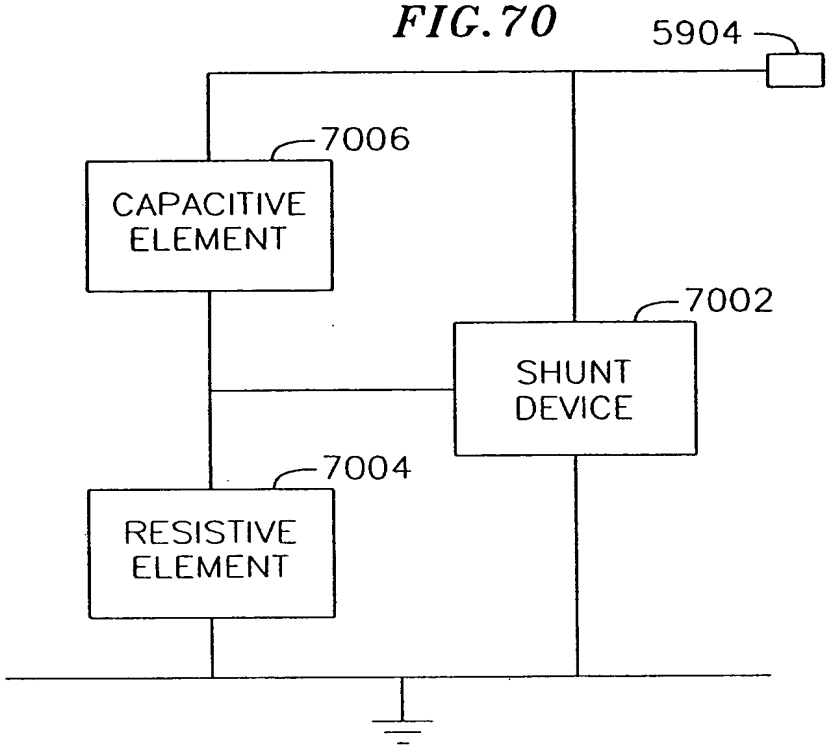

5904
7006
CAPACITIVE ELEMENT
7002
SHUNT DEVICE
7004
RESISTIVE ELEMENT

FIG. 71

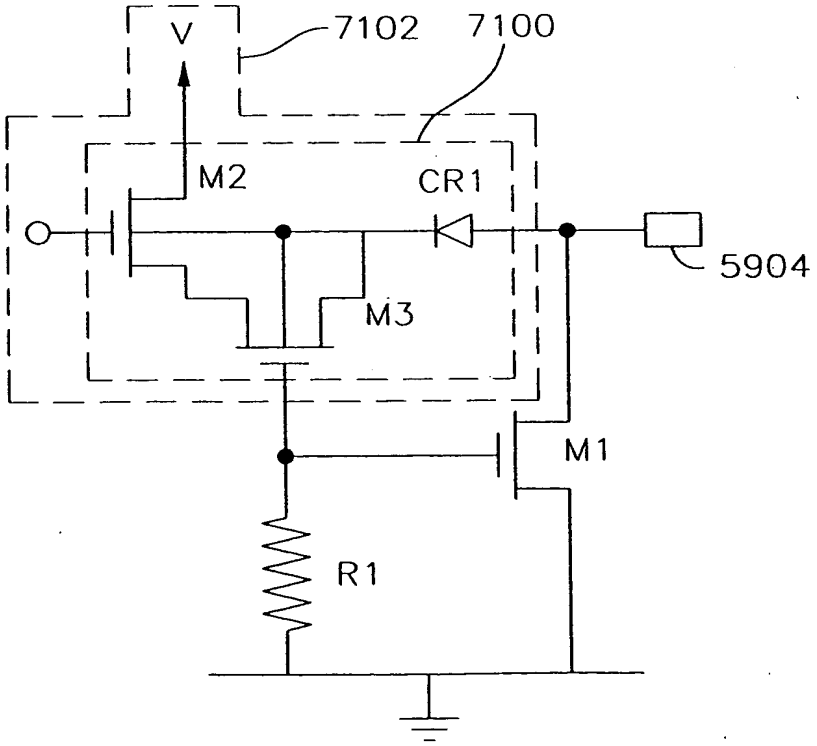

V
7102
7100
M2
CR1
5904
M3
M1
R1

FIG. 72

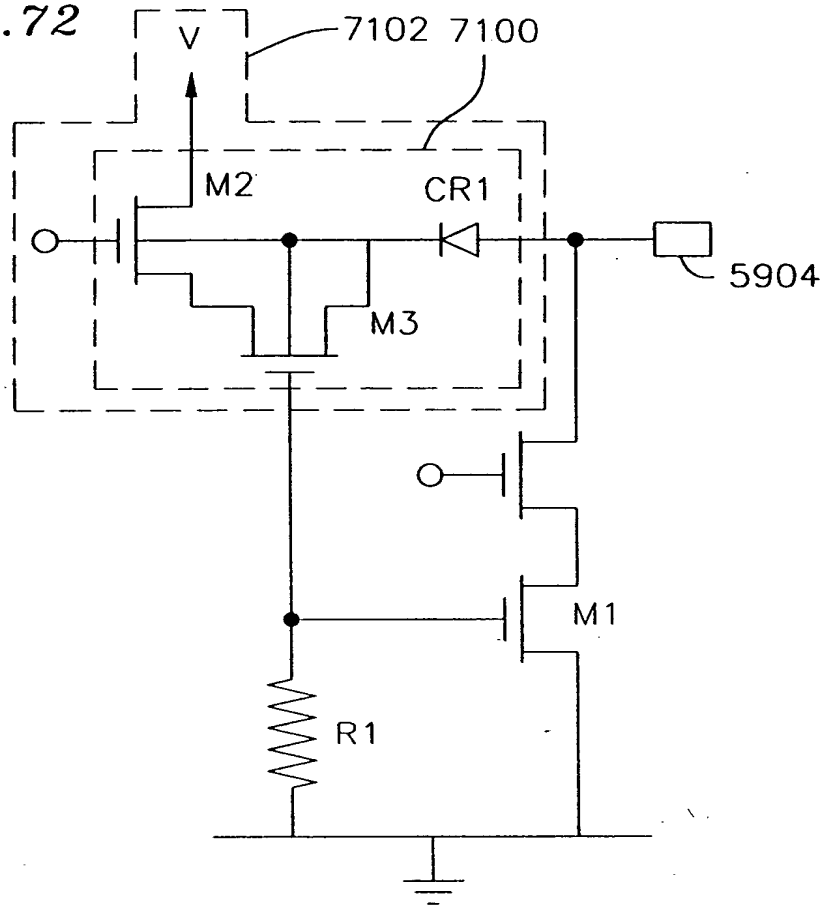


FIG. 73

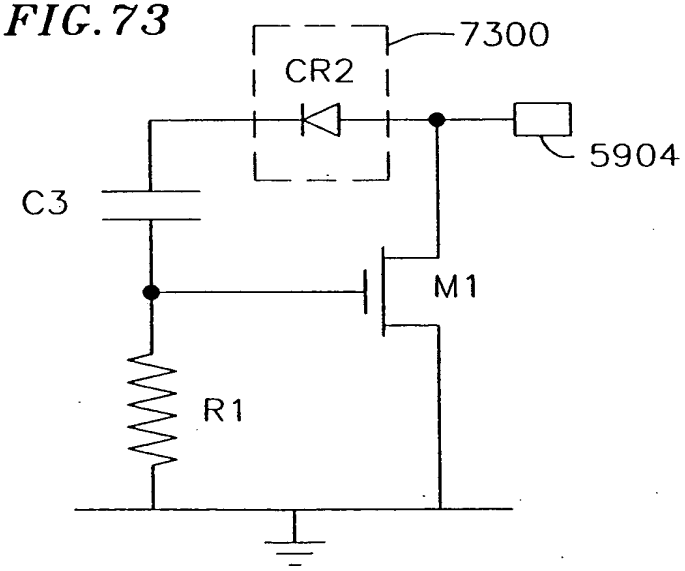


FIG. 74

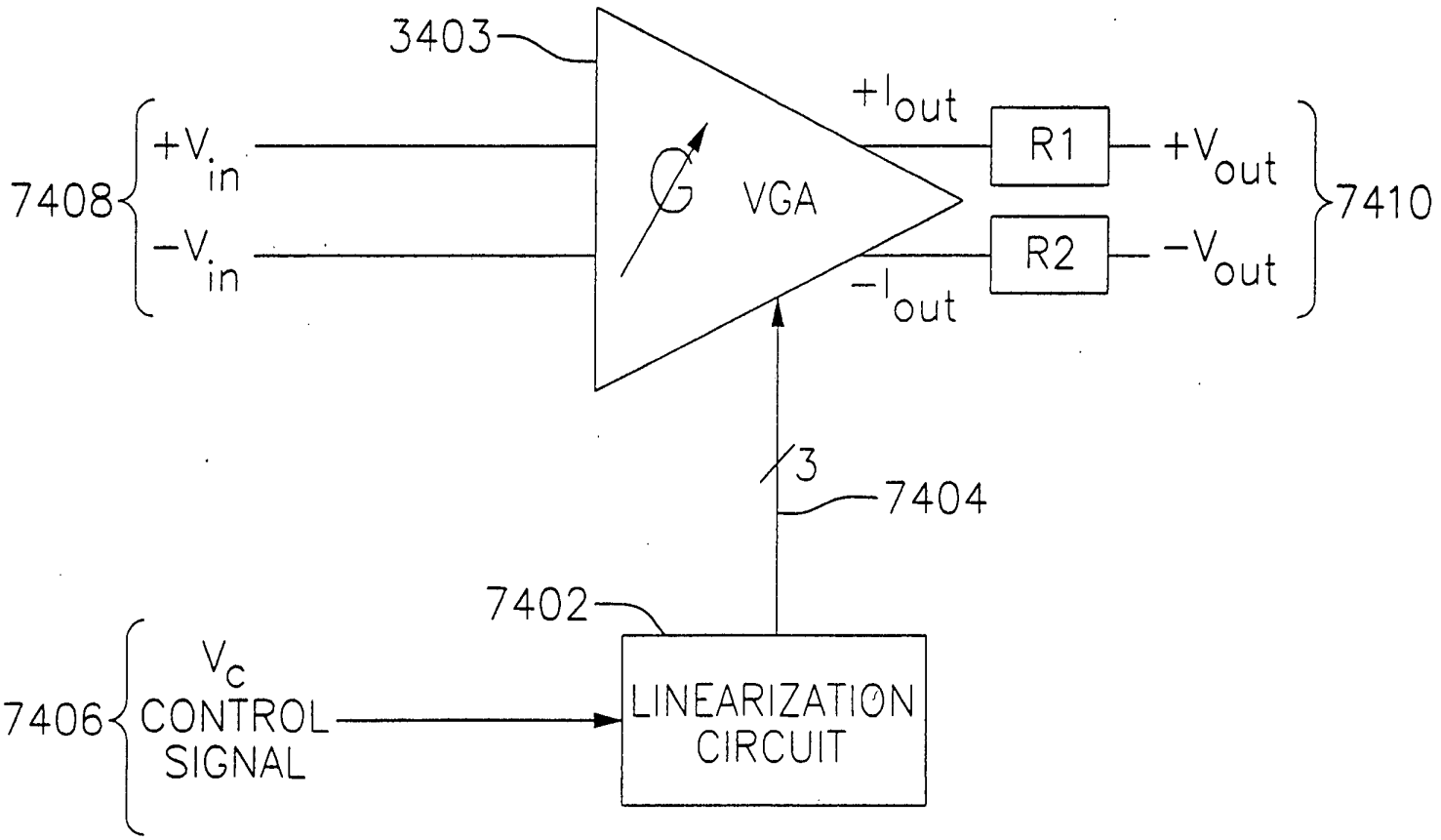

3403
+Iout
R1
+Vout
7408
+Vin
−Vin
VGA
R2
−Vout
7410
−Iout
3
7404
7402
Vc
CONTROL
SIGNAL
7406
LINEARIZATION
CIRCUIT

FIG. 75

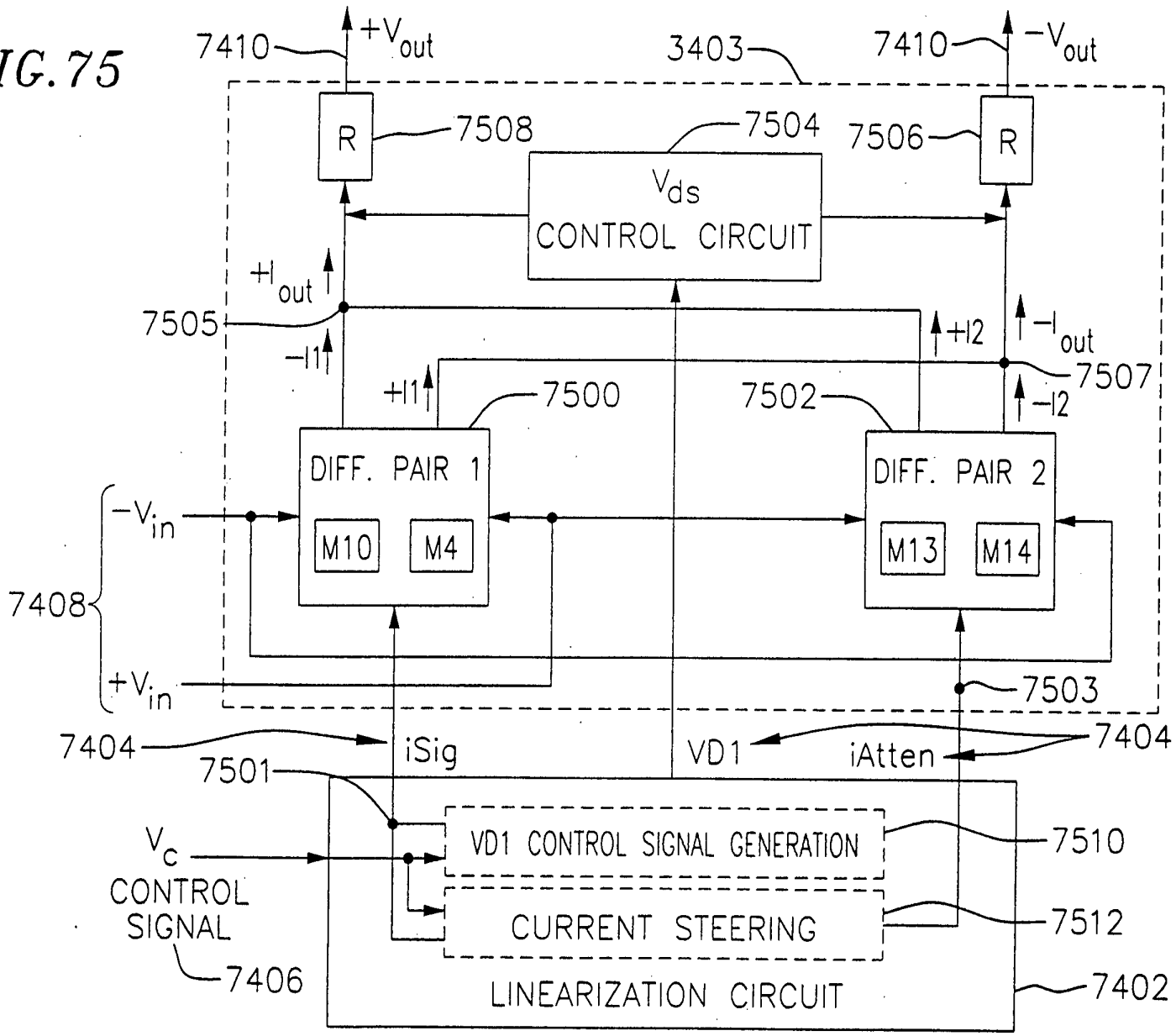

7410
+Vout
3403
7410
−Vout
R
7508
7504
7506
R
Vds
CONTROL CIRCUIT
+Iout
7505
−I1
+I1
7500
+I2
−Iout
7507
7502
−I2
DIFF. PAIR 1
DIFF. PAIR 2
−Vin
M10
M4
M13
M14
7408
+Vin
7503
7404
iSig
VD1
iAtten
7404
7501
Vc
CONTROL SIGNAL
7406
VD1 CONTROL SIGNAL GENERATION
7510
CURRENT STEERING
7512
LINEARIZATION CIRCUIT
7402

FIG. 76

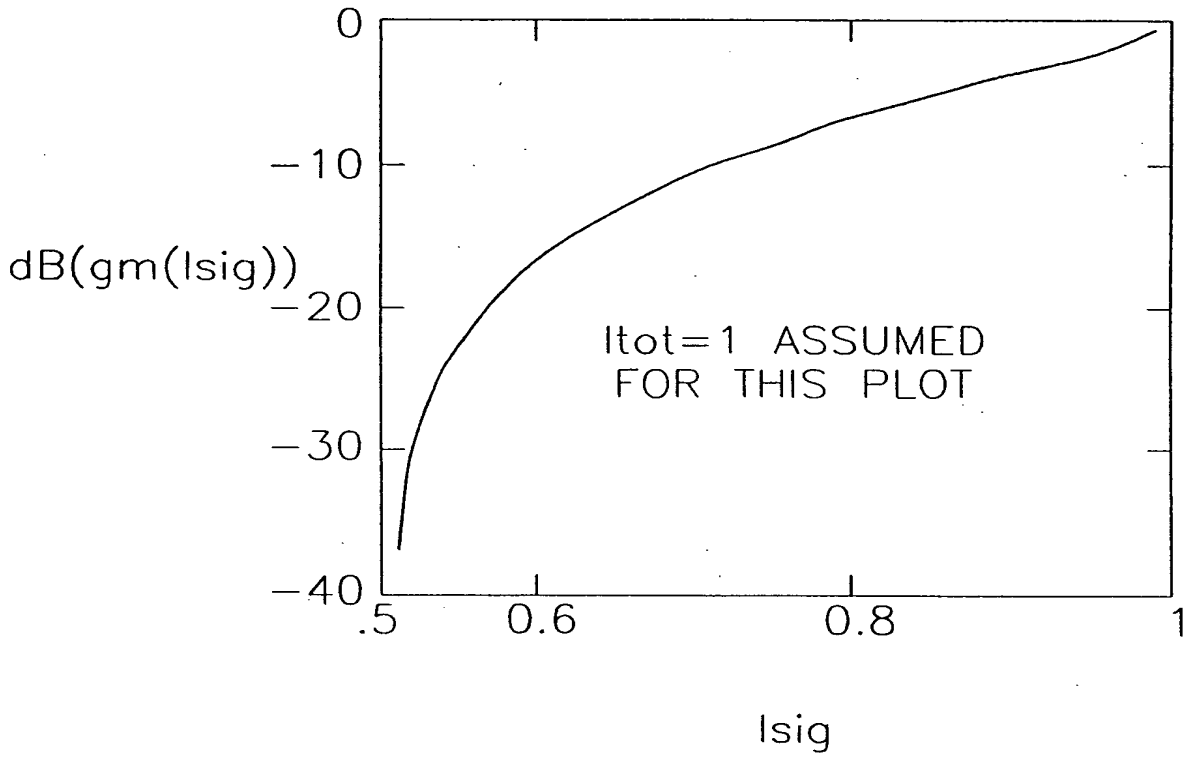

0
−10
−20
−30
−40
dB(gm(Isig))
.5
0.6
0.8
1
Itot=1 ASSUMED
FOR THIS PLOT
Isig

FIG. 77

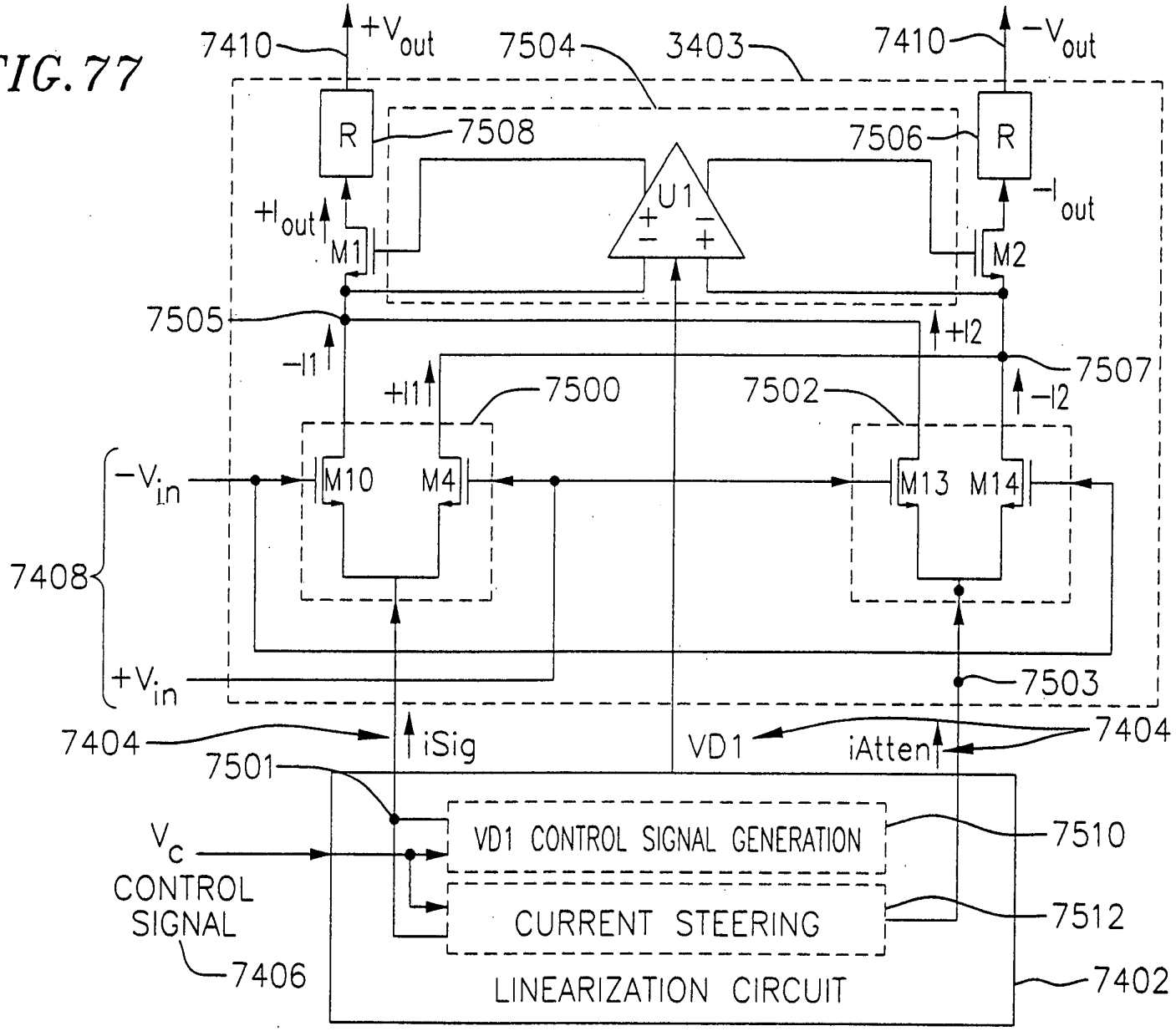

7410
+Vout
7504
3403
7410
−Vout
R
7508
7506
R
U1
+Iout
M1
M2
−Iout
7505
−I1
+I1
7500
7502
+I2
7507
−I2
−Vin
M10
M4
M13
M14
7408
+Vin
7503
7404
iSig
VD1
iAtten
7404
7501
Vc
CONTROL SIGNAL
7406
VD1 CONTROL SIGNAL GENERATION
7510
CURRENT STEERING
7512
LINEARIZATION CIRCUIT
7402

FIG. 78a

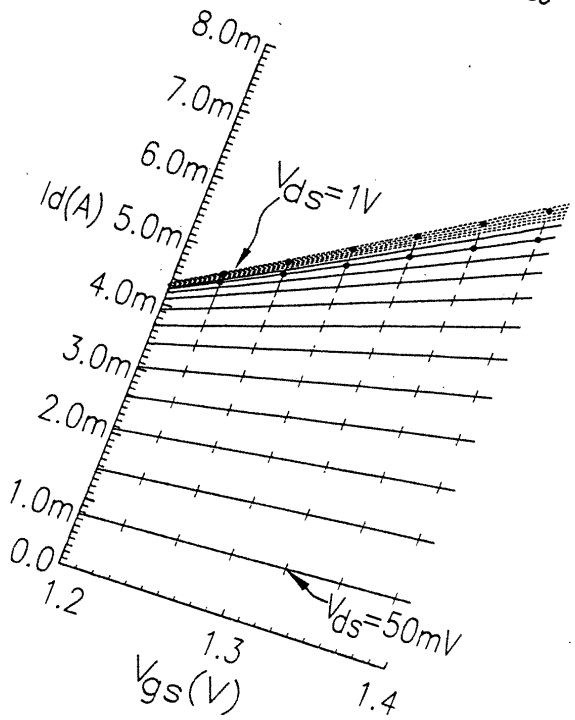


FIG. 78b

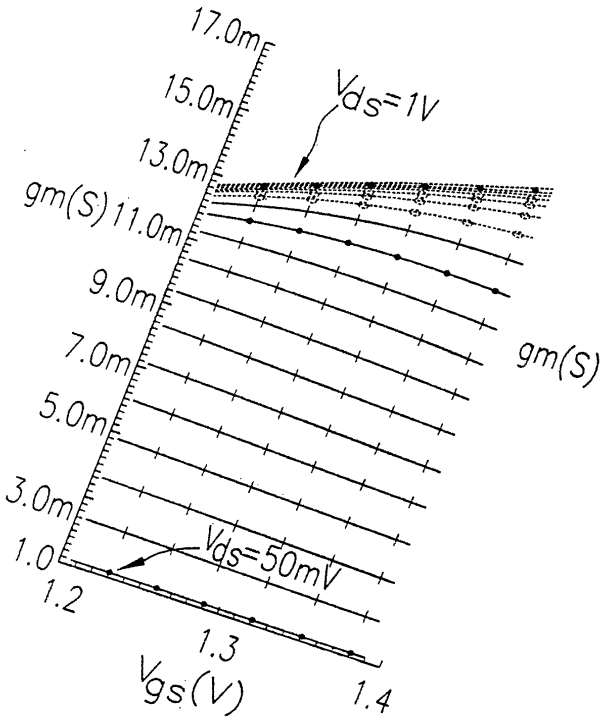


FIG. 78c

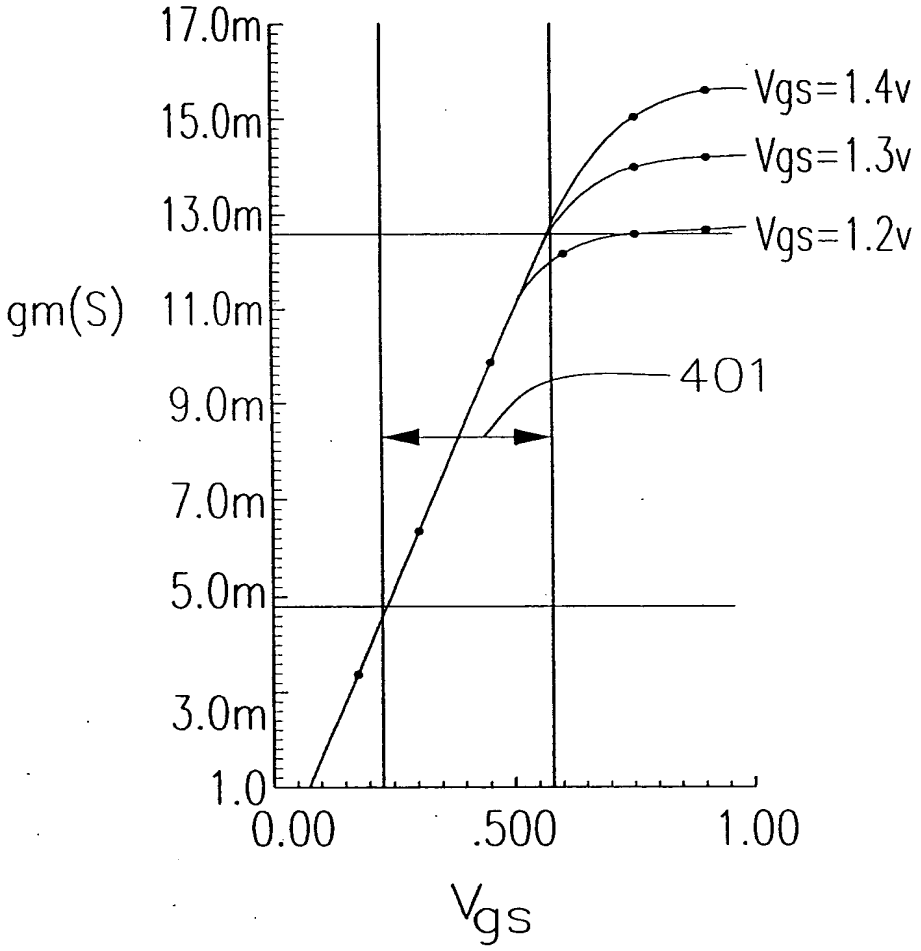

17.0m
15.0m
13.0m
11.0m
9.0m
7.0m
5.0m
3.0m
1.0
gm(S)
0.00
.500
1.00
Vgs
Vgs=1.4v
Vgs=1.3v
Vgs=1.2v
401

FIG. 79

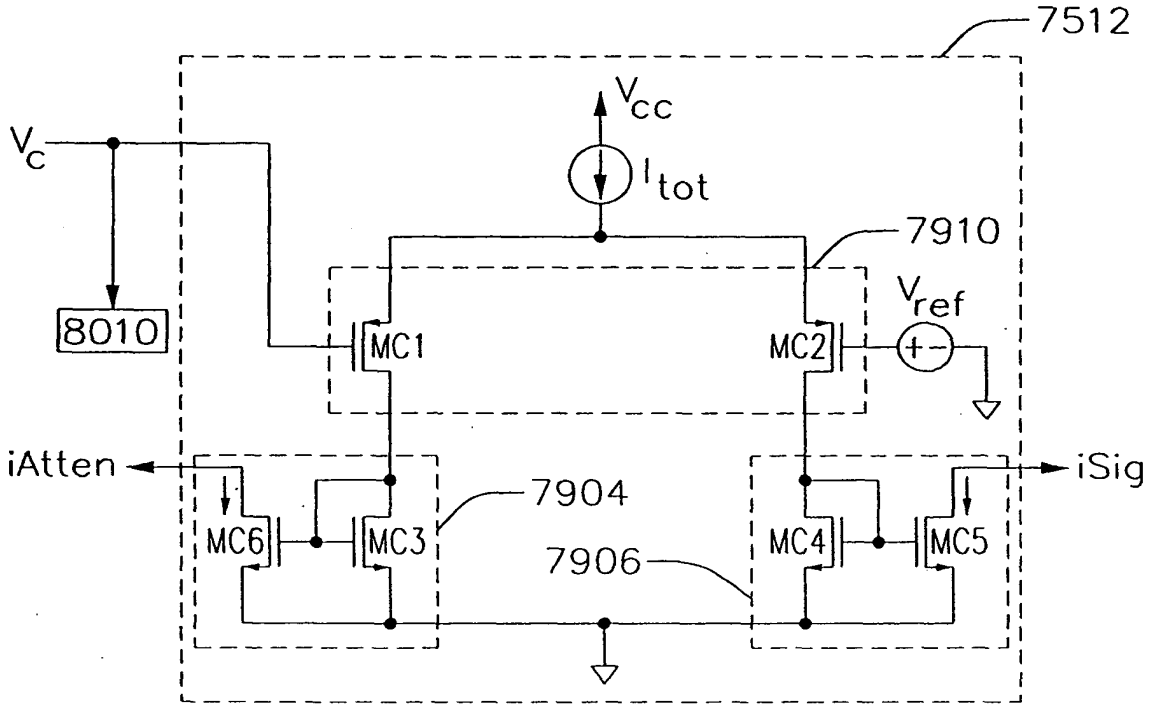
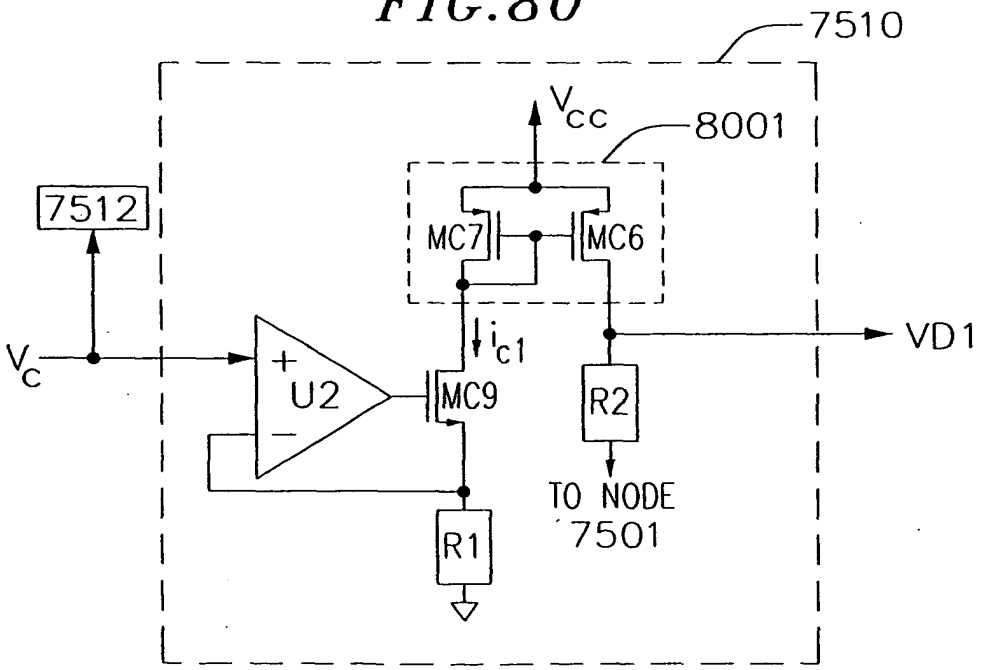

7512
V_{cc}
I_{tot}
V_c
7910
V_{ref}
8010
MC1
MC2
iAtten
iSig
7904
MC6
MC3
MC4
MC5
7906

FIG. 80


7510
V_{cc}
8001
7512
MC7
MC6
i_{c1}
VD1
V_c
U2
MC9
R2
TO NODE
7501
R1